GCE AS EXAMINERS' REPORTS

ELECTRONICS
AS

SUMMER 2019

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COMPONENT 1: PRINCIPLES OF ELECTRONICS

General Comments

This was the second examination of the new AS electronics component and candidates were more familiar with the longer responses needed for most questions and the extended written answers needed for the two QER questions. The examination proved accessible to most students and there were very few omissions of whole questions. The overall attempt rate was 97% or above. Statistical data showed that question 1 was the most accessible (FF84.3) with question 10 being least accessible (FF39.3). There were many very good responses to all questions. This report concentrates on highlighting those areas where notable errors were made. The marks ranged from 3 to 119.

Comments on individual questions/sections

Q.1 (a) & (b)

Both parts (a) and (b) were very straightforward and mostly answered correctly. For some reason a few candidates gave the EX-OR output to Q in the second table, but this was not a marking point.

(c) NAND replacement was generally well answered with occasional mixing up of OR and NOR. From most scripts it was clear to see which pairs of redundant gates had been identified. As always some crossed the first of the pair with the preceding gate in error.

Q.2 Many candidates found this question difficult (FF42.0).

(a) There are a number of ways of tackling this question. Few went for the straightforward method of inspection. Most used a variation of the voltage divider with varying degrees of success.

(b) The answer had to include ‘replacing’ one or two of the fixed value resistors with a variable resistor or potentiometer. Making R a different value or reversing the thermistor and R were answers seen quite often.

(i) The very high input impedance of the MOSFET makes the gate current effectively zero. Very few correct answers were seen. Most went for one of the currents from the diagram or table, or 0.06 A as the difference between them.

(ii) The equation from the data sheet had to be re-arranged to gain the first mark. The majority did this but then substituted the wrong data, the favourite choices being 24 V and 8 A.

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(iii) The simple approach to this is to use the $P = V_{OUT} x I_2$ version of the power equation with both values readily available in the table. Unfortunately, most went for $r_{DSon} = P/I^2$ and were then left with the problem of how to calculate P. Most selected the wrong values for I and V to substitute.

Q.3 (a) (i) As always candidates had great difficulty remembering Boolean identities and this was no exception.

(ii) Most correctly answered this but some, having achieved the correct EXNOR expression, went on to try to simplify further and forfeited the second mark.

(b) A few candidates did not realise that the whole point of the Karnaugh map is to produce as few groups as possible and, even when the map is correctly completed, they miss the group of 4 (C.A) and create only pairs or singletons. Provided that all the terms in the expression were then correct with respect to the map shown two marks were possible.

(c) Candidates were generally better at applying DeMorgan's theorem correctly than the subsequent simplifications. By far the most common mistake was to break the top bar but not keep the separate bars over the whole terms within the brackets. This results in (A.B) and ($\overline{A}$ + B).

Q.4 (a) Generally, the calculation was completed better than the circuit diagram. Many showed an input voltage to the Schmitt invertor or else connected R and C as a voltage divider across power rails. The capacitor had to be shown with a connection to zero volts (or very clearly implied). To gain the first calculation mark candidates had to select and rearrange the correct formula. As there are a number of RC formulae given in the data booklet a significant number picked the wrong version. The substitution required the correct multiplier to get the mark.

(b) (i) Numbers in the correct ratio (such as 750:250) also gained the mark but not 3 or 1:3.

(ii) As mentioned in part (a) incorrect versions of the RC formula were chosen by a number of candidates particularly T = 1.1RC.

(c) There were a lot of guesses, even when (b)ii was correct. The fact that only one mark was available should have been a clue that a repeat of the calculation in (b)ii, using the t_H formula, was not required but that a simple multiple of the answer above was needed. Unfortunately, many guessed multiply by 3 instead of 2.

Q.5 (a) Often the circuit diagrams were generally rather poor, particularly with the output part of the circuit, with many candidates not knowing the circuit symbol for an LED. The orientation of the LED was also problematic, and many ignored the instruction to use the Q output. Several candidates connected the S and R directly to the power rails.

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(b) Mostly very well answered and nearly every candidate achieved at least one mark due the ecf mark for $\overline{Q}$.

(c) As the question hints it is undesirable for both inputs to be at logic 0 at the same time. However, it is possible, and so the correct answer had to state that both outputs are forced high (logic 1). Disallowed, forbidden, flashing etc did not gain the mark.

Q.6 (a) (i) The value RC=0.47[s] shown or implied gained the first 2 marks. Some candidates provided the full exponential calculation which is risky but gives the correct answer. Using ln2RC is much easier.

(ii) Considering the difficulty of selecting and using the correct exponential formula there were a lot of correct answers seen. Answers of 1.4 V (12-10.6) were given one mark as, although the wrong formula was used, the difficult exponent part had been dealt with correctly.

(b) Very few candidates mentioned debouncing the switch. Many attempted to describe the action of the circuit often suggesting a 15-minute delay. Other answers suggested an analogue to digital conversion (even though the input is a switch) or a circuit to reset the system.

(c) Mostly correct. The first box had to be interrogative with either 'Is/Does count =50' or 'count =50?'. Not credited answers include 'Count =50', 'Have 50 people entered?', 'Let count =50' or 'Count>50?'.

Q.7 A very straightforward question with most candidates obtaining good marks (FF71.5). Mistakes include:

(a) Gain = 8 but ecf allowed on V_{IN} (max).

(b) Graph curving up to saturation

(c) Incorrect calculation of V_{OUT} (max)

Most graphs were drawn to an acceptable standard.

Q.8 (a) (i) Generally good, a handful divided 12 by root 2 in error.

(ii) A number of candidates ignored their previous answer and went back to use 11.3 or 12 V. This cost them the first mark.

(iii) Most selected the correct equation but then some used 1 instead of the current I, and others halved the frequency to 25 Hz.

(b) This was the second electronics paper with QER (quality of extended response) questions and so candidates were more familiar with the format. For this question answers had to include a full analysis of the zener diode regulator circuit and relate this back to all three points in the specification given. Faults needed to be identified, corrected and improvements suggested where appropriate.

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Higher tier answers were expected to state that the zener diode fixed the output voltage at 8.2 V provided the 10 mA current was present. Then calculate the current in R and the power dissipated in the zener diode (no load), taking account of the 10 mA and load current. This revealed that the current through R was too low and hence the output voltage might fall below 8.2 V. The power was also above that specified. One solution was to reduce and calculate a new value for R, with the top candidates realising this exacerbated the power overload problem. A zener diode with a higher power rating, or lower minimum current was then needed. Other acceptable approaches included assuming the 70 mA current and working backwards through the points.

Answers covered the whole spectrum of possible responses. It was quite common to not make any reference to the first point in the specification, relating to the output voltage, and many reduced R without calculation or noticing its impact on the power. A few candidates tried to apply Theverin's theorem to the circuit.

Lower tier answers often contained errors and only dealt with one point correctly or made two partially correct observations.

Q.9 (a) Well answered.

(b) Some candidates attempted to use multiple gates or took the outputs from below the LEDs, hence, always at 0 V.

(c) (i) Very few correct answers.

(ii) As so few realised the BCD counters reset automatically on the 10 pulse it was not surprising that the simple link from D to clock 2 was missing. Many answers had wires from every possible output of the counter, including from between the counter and gate, often with multiple logic gates.

(iii) About 50% of candidates assumed that the counter displays were in the same order as the denary number.

(d) Generally, a good response with a few attempting to use HEX for the second answer.

Q.10 This proved to be the most difficult question on the paper with a mean mark of 6.3 out of 16 and a high standard deviation. It is not clear why this was the case as the question is examining a basic transistor switching circuit and relay. The graph and diagram were particularly poor.

(a) A standard transistor question but with no scaffolding offered to the candidates. Most were able to gain marks for the individual parts. It was common for the final +0.7 V to be missing. A few subtracted 0.7 V from 12 V at the start.

(b) Very few candidates knew the form of the voltage transfer characteristics for a transistor, with a positive slope being favoured. Therefore part (ii) was often awarded as an ecf.

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(c) There were alternative approaches to answer this question. Collector current can be calculated by deduction, the voltage read from the graph in (b)ii from 12 V and dividing by 168 or by calculating the base current and using the h_{FE}. If the later method was used the 0.7 V was often neglected. When calculating the power V=3 V was often used instead of the value from (b)ii.

(d) Very few four-mark answers. Circuit diagrams were rarely of a standard expected at AS level. Many diagrams linked the DC and AC circuits. The diode, if drawn at all, was often across the collector and emitter. Very few correct symbols for the LDR and often in the wrong position.

Q.11 (a) The requirement to draw a circuit diagram of an op-amp voltage amplifier is a routine question. Although many did draw it correctly a significant minority repeated the same basic errors that occur every year, namely, wrongly identified type of amplifier, positive feedback and/or resistor values less than 1 kΩ.

(b) Most candidates gave good responses, but many wanted to change the slew-rate as well as the other two parameters. The slew-rate is a property of the op-amp (component) not the amplifier built from it.

(c) The second QER question had three main areas to be address in answer:

- Experimental method,
- Handling data
- Analysis and extra detail.

Higher tier (5-6) answers contained comprehensive information for all three section. Middle tier (3-4) answers covered at least two of these areas well but tended to omit some important details. Lower tier (1-2) answers had two to three correct details but were incorrect in places or had significant missing information. Most candidates referred to the definition of bandwidth correctly. Details and use of the measuring equipment were not particularly good although some did attempt to draw a diagram of the set up. Many implied rather than stated that V_{IN} was kept constant (one method). Similarly, many forgot to say that the frequency was varied and were ambiguous as to whether they were changing the frequency or amplitude of the input. It was unclear whether they were dealing with AC or DC signals. Better answers explained that clipping distortion had to be avoided with some using data from the previous parts to predict the behaviour of the amplifier.

Summary of key points

- For a multi-part numerical question each individual calculation should be clearly identified with quantity, equation, substitution, calculation, answer and unit.
- Candidates need to take greater care drawing diagrams, including electronic symbols and their connections being clearly shown.
- Where the evaluation of a system is required candidates should check that they have addressed every point in the specification. They need to show all appropriate calculations and compare the outcome with the specification and comment on the comparison.

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- When finding resistor values the ideal value calculated should be used unless the question has specifically asked for the preferred value from the E24 series.

- Thirty-five percent of the marks are for recall of knowledge so learning the basics such as Boolean identities and the transfer characteristics of components or subsystems is needed.

- Eleven of the equations given in the data booklet contain RC. Candidates should make sure they learn which one to apply in a given situation.

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COMPONENT 2: SYSTEM DESIGN AND REALISATION TASKS - NEA

General Comments

Centres are to be congratulated for their effort in presenting candidates' work for moderation, including the online recording of centre marks.

The assessment of the work was within tolerance in the vast majority of centres but in a small number of centres adjustments to marks were required.

In the majority of centres candidates produced a good range of tasks. Candidates should focus on a problem to analyse to enable them to write a design specification based on a specific identified problem.

Many candidates struggled to provide meaningful parameters and simply quoted power supply values, current consumption and cost without any justification. A full specification should include measurable parameters and numerical data.

The majority of centres provided excellent photographic evidence, but annotation of candidate's work was quite limited. A large number of centres failed to provide any annotation.

In all three tasks the main weakness was in the Evaluation section. To gain the full range of marks for the evaluation candidates must make valid critical and objective evaluation of performance. The evaluation should compare the system against the design specification and make suggestions for improvement to access the full range of marks. The suggestions for improvement must be relevant.

The consequence of not having many measurable parameters in the specifications resulted in some simplistic evaluations.

Most candidates provided relevant test results but there was little evidence of analysis of these results.

Comments on individual questions/section:

Task 1

The range of digital tasks was much better this year, with most centres taking on board the advice that the task should be based mainly from the logic and/or sequential logic systems topics within the specification.

In a small number of centres a few candidates attempted a task based on either 555 monostable or astable circuit. As previously stated this approach would not normally provide sufficient scope to allow candidates to access the full range of marks available.

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The accounts provided for the sub-system testing tended to be observational with very little recording of the testing that took place. For each sub-system a test reading should be provided with the output activated and non-activated.

Candidates in several centres produced outstanding digital tasks which could easily have provided the basis for an A level extended task.

Task 2

Unfortunately, a significant number of centres did not heed the advice that analogue systems should normally contain both an analogue input and an analogue output. A task based on a comparator, or a monostable/astable circuit is not appropriate. A small number of centres seem to think that connecting a transistor switch to the output of a logic gate constituted an analogue system.

The focus provided for an amplifier based tasked was an improvement on last year with a number of candidates providing an investigation of both gain and the frequency response of an amplifier.

To access the full range of marks for system realisation the use of an oscilloscope would normally be required for testing an analogue system. Although the results of simulation tests might prove to be useful for comparison, frequency measurements must be taken from the physical circuit.

Task 3

Candidates produced a very good range of tasks. Some of the work was outstanding and demonstrated considerable innovation.

For the microcontroller task at AS level, candidates are required to program the microcontroller via a flowchart program, other programming languages are not acceptable.

It is important that the flowchart diagrams included in the reports are large enough to enable the commands to be read.

To gain the full range of marks for system development, simulation tests should be carried out for the flowchart program. There is no benefit in downloading a program to a microcontroller until the flowchart is performing as expected. Screenshots of the simulation tests would be helpful.

Summary of key points

- Candidates' tasks should focus on a problem to analyse to enable them to write a design specification, including measurable parameters and numerical data.
- Evaluation must make valid, critical and objective evaluation of performance against the design specification.
- Digital tasks should be based mainly from the logic and/or sequential logic systems topics within the specification.
- Analogue tasks should contain both an analogue input and an analogue output.
- Microcontroller task at AS level, requires candidates to program the microcontroller via a flowchart program, other programming languages are not acceptable.

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