GCE A Level Examiners' Report

Electronics

A level

Summer 2026

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Introduction

Our Principal examiners' report provides valuable feedback on the recent assessment series. It has been written by our Principal Examiners and Principal Moderators after the completion of marking and moderation, and details how candidates have performed in each component.

This report opens with a summary of candidates' performance, including the assessment objectives/skills/topics/themes being tested, and highlights the characteristics of successful performance and where performance could be improved. It then looks in detail at each unit, pinpointing aspects that proved challenging to some candidates and suggesting some reasons as to why that might be.[1]

The information found in this report provides valuable insight for practitioners to support their teaching and learning activity. We would also encourage practitioners to share this document – in its entirety or in part – with their learners to help with exam preparation, to understand how to avoid pitfalls and to add to their revision toolbox.

Further support

Document	Description	Link
Professional Learning / CPD	Eduqas offers an extensive programme of online and face-to-face Professional Learning events. Access interactive feedback, review example candidate responses, gain practical ideas for the classroom and put questions to our dedicated team by registering for one of our events here.	https://www.eduqas.co.uk/home/professional-learning/
Past papers	Access the bank of past papers for this qualification, including the most recent assessments. Please note that we do not make past papers available on the public website until 12 months after the examination.	Portal by WJEC or on the Eduqas subject page
Grade boundary information	Grade boundaries are the minimum number of marks needed to achieve each grade. For linear specifications, a single grade is awarded for the subject, rather than for each component that contributes towards the overall grade. Grade boundaries are published on results day.	For unitised specifications click here: Results and Grade Boundaries and PRS (eduqas.co.uk)

[1] ***Please note that where overall performance on a question/question part was considered good, with no particular areas to highlight, these questions have not been included in the report.***

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Exam Results Analysis	Eduqas provides information to examination centres via the WJEC Portal. This is restricted to centre staff only. Access is granted to centre staff by the Examinations Officer at the centre.	Portal by WJEC
Classroom Resources	Access our extensive range of FREE classroom resources, including blended learning materials, exam walk-throughs and knowledge organisers to support teaching and learning.	https://resources.eduqas.co.uk/
Bank of Professional Learning materials	Access our bank of Professional Learning materials from previous events from our secure website and additional pre-recorded materials available in the public domain.	Portal by WJEC or on the Eduqas subject page.
Become an examiner with WJEC.	We are always looking to recruit new examiners or moderators. These opportunities can provide you with valuable insight into the assessment process, enhance your skill set, increase your understanding of your subject and inform your teaching.	Become an Examiner | Eduqas

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Executive Summary

The mean marks in all 3 components of A level Electronics this year, were slightly lower than in 2025. Analysis of responses to questions showed the level of difficulty of both exams to be similar to 2024 and 2025.

Component 1 & 2 exams

Both exams covered all assessment objectives and included questions on all topics of the specification. Both included synoptic questions, requiring candidates to draw together knowledge from both components. The level of demand was comparable with previous years.

Many candidates showed a high level of knowledge and preparation. As in previous years, most candidates performed well in calculations. Diagrams were generally well drawn though some graphs were poor. There was some improvement seen in written explanations although a significant number of candidates were unable to give clear, logical explanations.

In Component 1, candidates performed well in questions on combinational logic, passive filters and communication systems. In Component 2, questions on sequence generators, 555 astable, PCM and microcontrollers were answered well.

In Component 1, lower marks were gained in questions on the difference amplifier, transistors and comparators. In Component 2, low marks were gained in questions on RC networks, zener voltage regulators, PCM systems and design of a Schmitt trigger.

As in previous years the lowest marks in Component 2 were for the QER question, involving evaluation of a mixer. In Component 1 this year, marks in the QER question, while amongst the lowest, were similar to other low scoring questions. A wide range of marks were gained in the QERs. Some candidates gave an excellent analysis, evaluation and solutions while some were unable to analyse circuits.

The A level Electronics eBook includes examples and exercises on all topics. This is available on the resources section of the AS/A level Electronics webpage.

Component 3 NEA

For the first time this year, NEA samples were submitted electronically by centres, via the IAMIS system. Centres are thanked for preparing well-organised samples and correctly uploading them by the submission deadline. It should however be noted that each sample should be uploaded as a single pdf document.

The Electronics Task Forms were revised this year to add codes, identifying each of the marking criteria. Clear annotation on the Task Forms and scripts is very helpful in justifying marks awarded. The revised forms are available on the Electronics webpages under 'NEA'.

The marking criteria were well understood and applied accurately by most centres. Mark adjustments were required for a small number of centres.

Some outstanding projects were seen however in a few centres, work was below A level standard. A good range of tasks was produced by most centres. Designs must be based on an individual problem, matched to the candidate’s ability. Specifications should give realistic, measurable parameters. Subjective specifications, with few specific parameters, often resulted in simplistic evaluations. Centres should refer to their moderator’s report for specific feedback.

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ELECTRONICS

GCE A level

Summer 2026

Component 1 – Principles of Electronics

Overview of the Component

The examination paper covered all assessment objectives AO1, AO2 and AO3 as well as coverage of content across the component 1 specification. The standard was in line with previous years.

Many candidates' responses showed a high level of preparation for the examination, and a high level of knowledge was evident for many. Calculations were usually well laid out and easy to follow. Circuit diagrams were mostly well-drawn and accurate although some graphs were of a poor quality. There was improvement in many of the written responses by candidates although a significant number of candidates struggle with explanations.

There was a wide range of responses to the QER question 3(b), covering the whole mark range. Whilst many candidates answered this question fully with excellent analysis, evaluation and suggestions for solutions there were some who provided solutions but no evaluation whilst others were unable to analyse the logic circuit.

The questions 3(b) and (c), 10(a) and (d) contained synoptic material. Many answered all of these questions successfully indicating a good holistic understanding of the specification. The detailed analysis of the zener diode in question 10 caused difficulty for some candidates.

Candidates performed particularly well in the following questions:
Q1,2 and 2 on logic gates and combinational logic
Q6 on passive filters
Q11 on communication systems.

Many struggled with the following questions:
Q3 the evaluation of a complete system (QER) and synoptic microcontrollers
Q5 on the difference amplifier
Q7 on transistors
Q10 the comparator.

Comments on individual questions/sections

Q1 Straightforward and very well answered.

Q2 Straightforward for many but issues for some.

Whilst the majority of candidates answered this question with confidence, there were some who lacked an understanding of Karnaugh maps and/or Boolean algebra.

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Q3 Some excellent QER responses. Some incomplete responses.

This question contained the QER and a synoptic element. In part (b), the QER question, many candidates produced a good and thorough evaluation and identified many of the possible improvements. However, too many were focussed solely on the improvements and ignored the important part of evaluating all elements, identifying whether they meet the specification or not. For some, their marks were limited by not identifying the error in the astable which restricted them to the lower level of marks.

Part (c) was a synoptic element and was generally well answered showing good cross specification knowledge.

Q4 Most candidates showed a good understanding of the non-inverting amplifier. Marks usually lost on the frequency response and slew rate.

Parts (a) and (b)(i) were very well answered, although it was common for candidates to lose a mark for using a poor scale on the y-axis. Marks were lost in (b)(ii), the graph of the frequency response or in (c). Some candidates did not know the graph shape or the relationship between break frequency, gain and bandwidth in (b)(ii). In (c) many candidates failed to convert the slew rate to seconds and missed that they needed to calculate V_{IN} from V_P.

Q5 Many candidates answered this question poorly with the average mark being 6.7 out of 12.

A surprising number of candidates were unable to explain the necessity of balancing the bridge circuit in (a)(i). A disappointing number had difficulty calculating the voltages V_A and V_B which are straightforward voltage divider calculations. Similarly, a disappointing, smaller number, were unable to complete the difference amplifier circuit correctly in (b)(i).

Q6 Another very well answered question.

It was pleasing to see the large number of candidates that demonstrated an excellent understanding of filters both graphically and in the design of circuits. There were many clear, well drawn and accurate circuits.

Q7 There were many candidates that had difficulty with the second part of this question.

Nearly all candidates were able to complete parts (a) and (b) successfully. The longer multi-step calculation in part (c), though well done by many candidates, caused issues for others. Clear working made it possible to apply error carried forward (ecf) within the calculations.

Part (d)(i) caused difficulty for a significant proportion of candidates, with a lack of understanding of the shape of the graph apparent. The explanation in (d)(ii) was a clear differentiator between those who understood the transistor and those that didn't.

Q8 The excellent responses by many to this question demonstrated an improvement in the understanding of wireless communications.

Where issues occurred, it was in part (a)(ii) and (iii). Candidates were unable to calculate the minimum voltage for the given depth of modulation and/or were unable to draw an accurate sketch of the waveform produced. Again, ecf was important here.

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Q9 A polarising question. Candidates either knew the circuit or not.

The use of a ruler to ensure that the circuit diagram is clear, would benefit candidates.

Q10 Part synoptic, the explanations in parts (b) and (d) caused most issues.

Part (a) was well attempted by many but some were unprepared for the application of the zener diode. Candidates need to have knowledge of the whole specification for each component exam. Candidates that dropped marks tended to do so because of poor explanations in parts (b) and (d). These explanations need to link the calculations to the behaviour of, in this case, the op-amp in the comparator circuit.

Q11 Most candidates demonstrated an excellent understanding of communication systems.

Most candidates were well prepared for the calculations in this question. The main problem was the selection of the correct output power for the SNR calculation; ecf was applied to this part.

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Component 2 – Application of Electronics

Overview of the Component

Questions covered all topics in the Component 2 specification and addressed all assessment objectives. Questions 1, 2, 4, 7 and 9 included synoptic elements of assessment. The level of demand of the paper was comparable with that in previous years.

Many candidates performed well in calculations, showing intermediate steps and evidence of knowledge of multipliers. Answers often included well-drawn diagrams, usually in pencil to illustrate significant points. However, phrases used in some candidates' answers revealed a loose grasp of fundamental concepts. For example, 'voltage is sent through the resistor' and 'period = 2.18 Hz'.

While presentation was generally good it was very difficult to read some candidates' handwriting. The performance of some candidates could be improved by reading the question carefully, planning their response and checking what they have written.

Overall, the standard of answers was high. A particular strength was the performance in question 8, the microcontroller question.

Most candidates performed especially well in the following questions:
Q1 analysis of a sequence generator
Q2(c) calculations relating to a 555 astable
Q4(a) demonstrating PWM and PPM
Q8 the microcontroller-controlled game.

The following questions were less well answered:
Q2(b) behaviour of a RC network
Q3(b),(c) calculations relating to a zener voltage regulator and power supply
Q4(b) the structure of a PCM communications system
Q5(b)(ii) the design of a Schmitt trigger
Q9 concepts involved in the design and performance of a PA system.

Comments on individual questions/sections

Q1 The question was generally well answered.

In part (a), some diagrams showed a lack of planning (and an eraser!) Some failed to use the correct symbols for logic gates, especially on the input D_A. Some felt an urge to connect the Q-bar outputs to the corresponding data input. An alternative available for D_A was using De Morgan's theorem to give $D_A = \overline{A}$ **AND** $\overline{B}$.

In part (b), the main sequence was usually correct, but a minority made the odd mistake in the sequence of unused states. There were quite a few mistakes in (b)(iii), though most candidates identified the period of the clock. Parts (iv) and (v) were nearly always correct, including the Karnaugh maps.

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Q2 Part (a) was generally not well-answered. In part (ii), good answers made clear the meaning of latching and identified the latching combination.

In (b), the time constant and the half-life were usually correct. Candidates should have pre-planned their answers to (b)(iii). Good answers showed four distinct stages – the initial state of the LED, the time to charge to 6 V, the effect on the LED and then its subsequent behaviour.

In (c)(i), a number of candidates used the wrong formula, (usually T = 1.1.R.C) and gained no marks. The mark:space ratio in (ii) should have been expressed as a ratio, rather than a pure number.

Q3 In part(a)(i), the vast majority calculated the rms voltage correctly. In (ii), however, some graphs showed no evidence of rectification at all. Some lost a mark in (iii) for not labelling the peak value of V_{OUT}, likely a case of not reading the question.

In part (b), many made mistakes in calculating the maximum current through the resistor, but application of ecf meant that they did not lose marks in subsequent calculations.

Part (c) really required candidates to plan their answers and recognise the main stages of the calculation – calculate the minimum voltage across the resistor, hence obtain the minimum current through it, recognise the requirement of the zener and finally obtain the maximum available output current.

There were few fully correct circuit diagrams for the emitter follower in (d)(i). Incorrect transistor symbols and connections to the rest of the circuit abounded. Then in (iii), few could state the benefits of the emitter follower.

Q4 Part (a) was usually answered well, though some lost the odd mark for careless drawing. Use of a ruler would have avoided many of these losses. Many failed to recognise the correct blocks for the ADC and shift register in part (b).

In part (c), most recognised the effect of the reset, though some had this effect lasting only for one division on the time axis.

The other common error was to have the signals W, X, Y and Z change on the falling-edges of the clock pulses, (or on both edges, or just randomly!) Quite a few misunderstood the task of reading the output word in (iv), though ecf saved many.

Q5 In part(a), answers needed two clear parts – the meaning of ‘bounce’ and possible consequences of it. Again, answers could have been better planned.

Many answers to part (b)(i) were muddled, another case where careful planning would have helped. Around half of the candidates could design the Schmitt trigger in part (b)(ii), though rather more could complete the output signal. A common error was to use the 3 V switching thresholds on more than the two occasions.

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Q6 Most scored the mark for (a)(i) but then answers to (ii) were often too 'woolly'.

The required answer to part (b)(i) was simply that the lamp got dim, and many knew that. Much rarer was a convincing explanation as to why that happened. Part (iii) was usually correctly answered. In part (iv), many placed the label 'X' either on the sinusoidal sections of the trace or on the vertical sections and lost the mark. Many knew how to obtain the breakover voltage and how to describe the process. Most answered part (v) correctly.

Q7 Parts (a) and (b) were not well-answered by most. Vague statements abounded, and few candidates gave considered and accurate answers. Planning and careful checking were essential. In part (b), few were able to reason that the voltage at Y would rise.

A common misconception in (c) was that laser light travels faster than LED light! The peak power calculation in (d) was often successful.

Q8 This was the undoubted success of the paper for many. Parts (b), (e) and (f) were almost always correct. It was parts (a) and (g) that seemed to cause the problems. Once again, answering parts (c) and (d) required forethought and planning. Each of these parts required answers to the questions, "What happens if the switch is pressed?" and "What happens if the switch is not pressed?" It was often difficult to distinguish these.

Q9 In part (a), few identified the difference in performance of the two sub-systems. Part (b) proved equally difficult for some. Most gave correct answers to part (b)(i), but few gave clear and correct answers to part(b)(ii).

QER It was expected that most would recognise that the circuit diagram was incorrect and that the op-amp inputs needed reversing. Instead, many thought that the circuit was that of a non-inverting amplifier! They followed that with a calculation that gave the maximum voltage gain to be 11 and worried that that did not meet the specification.

In reality, one of the big challenges was to obtain a voltage gain of 0. Most recognised that the gain could not be controlled independently for the two inputs. Many suggested that the solution was to change the feedback resistor for a fixed resistor and change the input resistors to be variable. This did not solve the requirement for zero voltage gain. Better candidates suggested adding a potential divider to each input (and drew diagrams to illustrate the meaning).

Most candidates performed bandwidth calculations and deduced that the bandwidth would be well in excess of that specified in the specification.

In parts (d)(i) and (ii), many answers were unconvincing and vague. Part d(iii)I was often wrong but lead to ecf marks for part II.

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Component 3 – Extended System Design and Realisation Tasks

Overview of the Component

This component requires each learner to complete two tasks independently. The tasks build on the concepts studied throughout the specification and the requirement to relate practical circuit design and realisation to knowledge and understanding gained from the study of components 1 and 2.

Task 1 (20 marks) involves the development of a microcontroller system programmed through assembler language.

Task 2 (50 marks) is a substantial system development including analogue and digital sub-systems in an integrated design.

Each task enables learners to carry out a design and realisation task based on an individually identified problem, context or opportunity.

Centres are to be congratulated for their effort in presenting candidates' work online for moderation. The Electronics Task Forms have been revised with codes identifying the marking criteria however some centres used the old forms. Also some centres uploaded multiple pdfs It is now a requirement that each sample is uploaded as a single pdf document.

In most cases the marking criteria were understood well and applied consistently, with marking within tolerance in the majority of centres. In a small number of centres, adjustments to marks were required.

Both tasks:

- Design specifications need to be based on a specifically identified problem matched to ability and interests.
- Some specs were subjective.
- In a few centres the work was below A level standard.
- Detailed, realistic, justified and measurable specifications are still an issue.
- Not having many measurable specification parameters often resulted in some simplistic evaluations.
- Test result analysis was often very simplistic.
- Some images were lacking clarity.
- Improvement suggestions must be relevant and state why they would be beneficial.
- All components must be clearly marked with the correct names.

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Task 1:

- Flowchart annotations and predictions should be included.
- A few candidates used other programming languages such as Basic or generated their code from a flowcharting program. Neither are acceptable.
- Any commands given in the template cannot be included in the 10 required, unless used in the main program or subroutines.

Task 2:

- Some research was trivial and did not inform the specifications.
- Some sub-systems were trivial. Alternative sub-systems should be designed and investigated.
- All the sub-systems that interface with each other in a complete circuit should be tested.

Tasks
Comments on tasks/questions relating to candidate performance/meeting assessment criteria

In both tasks:

Candidates should focus on a problem to analyse that will enable them to write a design specification based on a specific identified problem matched to their ability and interests. It is unacceptable that all candidates do the same or very similar projects. This year, it was also noted that in a few centres the work was below A level standard.

Many candidates failed to provide meaningful specifications and simply quoted power supply values, current consumption, timings etc. without any justification. Detailed, realistic, justified and measurable specifications (at least two for task 1 and three for task 2) with tolerances (where relevant) need to be included. Where a full specification was included, this helped candidates access the full range of marks for the evaluation as they tested against their technical specification. A consequence of not having many measurable specification parameters often resulted in some simplistic evaluations.

Test results were often taken for the circuits but the analysis of these results was often very simplistic. The majority of centres provided excellent photographic evidence. However, some centres provided images of circuit layouts that tended to be lacking clarity to see any detail. Further photographic evidence, for example, showing testing, together with explanations should be included.

Improvement suggestions must be relevant and state why incorporating such an improvement would be beneficial rather than simply mentioning trivial points such as using more accurate resistor values, louder buzzers or an on/off switch.

Task 1

System Planning

Marks for quantitative design specification points should be based on analysis of the problem and contain detailed, realistic and measurable electronic parameters. Battery voltage without justification should not be considered a quantitative specification. The distance at which an LED can be seen is subjective and depends on the observer and therefore should not be considered a measurable electronic parameter.

Flowcharts and predictions should be included to aid understanding of the program.

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System Development

Most candidates wrote their own assembler programs, however, a few candidates used other programming languages such as Basic which are not acceptable. Also, some candidates generated their code from a flowcharting program. This too is unacceptable.

Note that credit cannot be awarded for commands used to configure the ports as these are given in the template. However, credit can be given should these same commands be used by the candidate in their main program and any sub-routine they write.

Candidates are required to provide 10 or more different commands to access full marks, in a lot of centres these were listed and this is good practice. Note that using the same command multiple times only counts as one.

System Realisation

All components must be clearly marked with the correct names and not left as generic names e.g. IC1 to gain the mark for an accurate circuit diagram.

Evaluation

Although a critical and objective evaluation was often provided, some were very simplistic and lacked detail. Often the problem was not including justified measurable parameters in the specification from which outcomes could be evaluated against.

Task 2

System Planning

Often marks were over awarded for qualitative design specifications. Specifications should be based on analysis of the problem and contain realistic and justified electronic parameters from research, rather than concentrating on component details which can be found in the course notes. As a result, some research was trivial and did not inform the specifications.

System Development

Candidates are required to use 6 or more different sub-systems. At A level the sub-systems are expected to consist of more than one component. An output together with a transistor would be classed as one sub-system rather than two. Switches should be tested with a logic gate rather than individually. Consequently, some candidates did not reach the required number of sub-system tests needed for the upper tier marks.

Test results obtained from circuit simulations are only valid if real components are chosen rather than the generic IC1 and Q1. Real components not only model real circuit behaviour but provide an accurate, high quality and fully labelled circuit diagram. Suitable values of resistors, connected in series with LEDs should be calculated and then tested by measuring the current. A lot of circuit simulations were observed which had the default 1k resistor with LEDs.

Alternative sub-systems should be designed and investigated and not simply mentioned to be credited. They should be a viable alternative and reasons given for choice.

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System Realisation

The physical circuit layout produced by most candidates was of a very good standard, with the majority of circuits constructed very neatly on breadboard, with horizontal and vertical wires not covering ICs or other components.

Although test results were often provided for the complete system, the analysis was generally limited. All the sub-systems that interfaced with each other in a complete circuit should be tested with a fully labelled complete circuit diagram included.

When testing, there should be evidence of tests carried out on the actual components used in the final design rather than generic simulation models. A lot of centres provided good photographic evidence of this, whilst a minority only showed simulations.

Evaluation

It is important to compare results with specifications and their tolerances and comment on this, rather than simply stating “the specification has been achieved”.

A consequence of not having sufficient realistic, measurable parameters in the specifications often resulted in some simplistic evaluations in a lot of cases.

Task marking
Comments on approaches to internal marking

If applicable, it is important that all centres action the advice given in their individual moderator reports.

Annotation on candidates’ work and task-lists was a great help in moderation. However, a large number of centres showed little indication on the task-list as to why marks were allocated and some did not show marks at the end of each section. Some ticked all points but did not give full marks for that section. It is good practice to indicate where (and possibly why) marks have been given (or not) and also reference it on the candidates’ work. This not only helps the moderation process but also benefits candidates by illustrating how and where they have achieved the criteria.

Candidates are not required to satisfy every individual bullet point within an assessment tier to access the marks. A holistic approach is taken when assessing these tiers; if a candidate has produced a circuit that worked consistently and reliably but has not recorded all of their testing, credit can still be given for this point. Further teacher annotation on the scripts as to where a circuit has been witnessed as working or where testing has been carried out, would aid the moderation process.

The range of tasks produced within most centres was very good. In some centres, candidates produced a very good range of tasks with some of the work being outstanding. In a small number of centres all candidates produced similar or very simple projects. It was also clear that some centres had prescribed possible tasks. Candidates should select their own focus for the tasks based on different, individual problems or interests and this is expected to produce a wide range of tasks within a centre.

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Supporting you

Useful contacts and links

Our friendly subject team is on hand to support you between 8.30am and 5.00pm, Monday to Friday.
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Email: electronics@eduqas.co.uk
Qualification webpage: AS/A Level Electronics

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