GCE AS EXAMINERS' REPORTS

ELECTRONICS
AS

SUMMER 2018

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COMPONENT 1

General comments:

This was the first examination of the new AS electronics component and whilst there were similarities to the old ET1 and ET2 there was significant new material and a much longer format, with fewer short response answers and the addition of two QER questions. The examination proved accessible to most students and there were very few omissions of whole questions. The marks ranged from the mid-teens to 119 out of 120.

Specific comments:

Q1. (a) The truth table was generally answered correctly with just a handful of AND or NOR outputs given for the NAND gate. Error carried forward (ecf) awarded for column Q.

(b) Pins 4 to 7 on the multiplexer were 'don't care' as C was connected to 0V and pins 0 to 3 were marked according to Q in the truth table. There were some surprising omissions for this part question. In part (ii) references to size or cost were not credited.

Q.2 (a) In the past candidates always seem to have had great difficulty remembering Boolean identities and this was no exception with frequent mistakes in both parts. A common error in (ii) was B + A even though a version of this type of expression is on the data sheet.

(b) A few candidates don't realise that the whole point of the Karnaugh map is to produce as few groups as possible and they managed to link 7 overlapping groups. However, the most common error was to miss the group of 4 ($\overline{C}.\overline{B}$). Provided that all four terms in the expression were present then correct two marks were possible.

(c) Candidates are generally better at applying DeMorgan's theorem correctly than the subsequent simplifications {see part (a)}. Where there are double errors that lead to a correct final answer no credit was given. By far the most common mistake was to miss of the brackets on the ($\overline{A}$ + B) term.

Q.3 (a) Both parts (i) and (ii) were very straightforward and many gained full marks.

(b) Unfortunately a handful of candidates ignored the fact they had produced a simplified expression in (a) (ii) and used part (a) (i) to draw the circuit diagram. This resulted in a mish-mash of over 10 logic gates and often difficult to follow interconnections. However, if it was correct then the marks were awarded accordingly as minimum gates was not requested on this occasion.

(c) Generally well answered with the caveat mentioned above. Error carried forward marks from (b) were applied.

(d) Most candidates found the explanation of the flow chart very straightforward. Marks were lost if the pulsing effect of the buzzer was unclear or the iteration until the belt was fastened was not mentioned.

Q.4 (a) The calculation of the short-circuit current is needed to calculate R_0 and many made a mistake at this point and divided 18 by the total resistance of 720Ω. Using the 160Ω resistor in the numerator of the potential divider equation when calculating V_{OC} was a common mistake.

(b) (i) Although generally straightforward errors included failing to label the circuit, using the supply voltage instead of V_{OC} and missing off the equivalent resistor or labelling it 120Ω.

(ii) Once again the potential divider equation caused a problem to weaker candidates with incorrect values used. Those that attempted the current approach sometimes used I_{SC} instead of calculating the new current using V_{OC} divided by the total circuit resistance. The parallel resistance mark was awarded if 120Ω was seen in any context.

Q.5 (a) This was the first time a QER (quality of extended response) question has been asked in an Electronics exam. Individual marks are not awarded for points made in the answer. The examiner reads the whole response and decided whether to grade it as top, medium or bottom tier based on the overall answer. Within each tier the final mark is chosen by considering both accurate and relevant factual content and the structure and coherence of the answer.

For this question answers had to include an analysis of the function of each part/subsystem of the circuit and relate this back to the specification given. Faults needed to be identified, corrected and improvements suggested where appropriate.

Higher tier answers probably discussed the roll of the pull-up and pull-down resistors in the input subsystems, identified the fault with the diode and corrected it and, hopefully, commented on potential problems with the light sensing subsystem, with the very top response discussing ways of conditioning the signal at A. Replacing the npn transistor with a MOSFET may be an appropriate comment if fully justified.

Lower tier answers often contained errors and only dealt with one point correctly (e.g. the diode) or made two partially correct observations.

(b) Many candidates were able to calculate the base current correctly but mistakes in the voltage drop across the base resistor, 11.6 instead of 10.9, meant the value of R_B came out as 4640Ω instead of 4360Ω. In part (ii) the preferred value had to be smaller than the answer given in (i). Many candidates chose the nearest value and went higher to 4.7kΩ.

Q.6 (a) The reading of the graph scale was rather poor for candidates at this level with many reading the resistance value at 30°C instead of 25°C. Very few used the simple ration method to find the V_T or R_V instead relying on the potential divider equation which often introduced errors. Error carried forward applied from incorrect R_T.

(b) Many candidates mentioned resistance changing with temperature without specifying thermistor resistance or the trend. Other answers were generic for comparators without relating the various voltage values to the temperatures in this application.

(c) One successful approach was to use the graph and hence calculate V_T values at 20 and 25°C and compare these with the value of V_X.

(d) A lot of very non-standard symbols were seen. A resistor between the comparator and gate is not needed but treated as neutral as $I_G \approx 0$.

(e) There were frequent mistakes with the calculation of the current with candidates using $P = I^2 r_{DSon}$, compounding the mistake by using 60W instead of 45W and not realising 27A was rather a huge value. However e.c.f on the g_m formula allowed some marks to be awarded.

Part (ii) had similar problems with current and many tried to use P=IV rather than $I^2 r_{DSON}$. Power greater than 100W should have sounded alarm bells.

Q.7 (a) There was generally a rather poor understanding of the theory of latching and 1's and 0's appeared rather randomly. The last line indicated an undesirable state but logic 0 at each NAND gate input forces both outputs high.

(b) The answer to propagation delay must relate a change in output to a change in input. Simple statements e.g. 'time for the signal to pass through a logic gate' are insufficient. A good number of scripts had an even number of NAND inverters and others did not connect both inputs together. The NAND inverter at the end was a high-level demand answer which a good number of candidates scored.

(c) A very straightforward question which was mostly answered correctly.

Q.8 (a) A straight forward select and use the formula question meant that many got the value of V_{OUT} correct although some omitted the sign.

(b) A challenging question on the application of a summing amplifier. A reasonable number spotted the inversion, fewer calculated the correct amplitude and only the top scoring candidates gave the off-set effect correctly.

Q.9 (a) (i) Use of f=1/RC scored no marks.

(ii) Many candidates calculated t_h and t_l correctly but did not express these as a ratio.

(iii) Diagrams often showed poor relationship to the scales and did not show exactly 2 cycles.

(b) Mostly very good answers for the counter diagram were seen. A few left off the first clock connection or connected Q to D.

(c) (i) Again mostly well answered with a handful selecting D and B as the inputs.

(ii) The marks for X and Y were readily obtained but a lot of scripts left the pulse 9 line blank. It should be a repeat of clock pulse 0.

(iii) The question asks about time whereas many answers were given in terms of pulse number. This often led to candidates making the mistake of giving X ON for 5 pulses instead of 6 seconds.

Q.10 (a) The diagram for the full-wave rectifier was very difficult to assess as any mistake makes the circuit unworkable. In order to give partial credit all connections were ignored when awarding the diode orientation mark. These connections were then assessed independently.

(b) Many stopped at $V_0 = 8.5\sqrt{2} = 12.0$. Others subtracted 1.4 first then tried to use the $\sqrt{2}$.

(c) Disappointedly very few scripts had both full wave rectification and labelled, reduced peak waves shown. Some candidates showed the ripple voltage on this diagram.

(d) For a large current the ripple should be significantly greater than one 2mm square. Rather poor-quality diagrams for both (c) and (d).

(e) There were a lot of mistakes in the voltage regulator circuit. These included: standard diodes rather than zener, incorrect orientation of the diode, no labelling, load resistor across power rails and missing series resistor.

Q.11 (a) This was generally well answered with most candidates deducing the gain of 24 and attempting a non-inverting amplifier. Those that did draw an inverting amplifier, with resistor values compatible to the gain they had specified, were able to score 2 marks for the circuit diagram. Unfortunately some candidates, whose answers initially looked good, had mislabelled the terminals of the op. amp hence giving positive feedback. This obviously lost them some marks.

(b) The remarks in the first paragraph of Q5a apply here and a holistic mark was awarded for QER.

Almost all candidates identified clipping distortion, and many were able to suggest ways of reducing it. Fewer candidates identified slew-rate distortion but those who did were usually able to indicate ways of counteracting the effect on the output signal. Many scripts used diagrams to illustrate answers.

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COMPONENT 2 – NEA

General comments:

Thanks are extended to centres for their effort in both organising candidates' work for moderation and the online recording of centre marks.

In the majority of centres candidates produced a very good range of projects. In a small number of centres it appeared that candidates had very similar design brief from which they developed their own set of parameters. The specification requires candidates to select their own focus for the tasks based on different problems and this is expected to produce a wide range of tasks within a centre.

The assessment of the work was within tolerance in the vast majority of centres with very little adjustment to marks required.

In all three tasks the main weakness was in the **System Planning** and **Evaluation** sections.

Candidates should focus on a problem to analyse to enable them to write a design specification based on a specific identified problem. Design specifications should contain a range of both qualitative and quantitative terms based on their analysis of the problem and contain detailed realistic electronic parameters.

The evaluation should compare the system against the design specification and make suggestions for improvement to access the full range of marks. Suggestions for further development must be relevant.

A significant number of candidates provided extensive test results but there was very little evidence of analysis of these results.

The majority of centres provided excellent photographic evidence but annotation of candidates work was quite limited.

Specific comments:

Task1:

Digital tasks should be based mainly from the logic and/or sequential logic systems topics within the specification to access the full range of marks. In a small number of centres all candidates attempted a task based on a either 555 monostable or astable circuit. This would not normally provide sufficient scope to allow candidates to access the full range of marks available for the digital task.

In contrast to this approach candidates in several centres produced outstanding digital tasks which could easily have provided the basis for an A level extended task

Task 2:

Analogue systems should contain both an analogue input and an analogue output. In a small number of centres all candidates attempted a task based on a light/temperature sensing sub-system connected to a comparator, with the sensing sub-system considered as “digital” input. To access the full range of marks for system realisation the use of an oscilloscope would normally be required for testing an analogue system.

The focus provided for an amplifier based tasked was often quite narrow with the gain formula being investigated for several combinations of resistor values.

It was also common to see the gain calculated at several frequencies well below a value sufficient to calculate the amplifier bandwidth.

To access the full range of marks an amplifier based task would normally require investigation of both gain and frequency response of the amplifier.

Task 3:

Candidates produced a very good range of tasks. Some of the work was outstanding and demonstrated considerable innovation.

For the microcontroller task at AS level, candidates are required to program the microcontroller via a flowchart program, other programming language such as C or assembler are not acceptable.

In many cases the flowchart provided in the report was far too small making it very difficult to read the commands.

A small number of centres allowed task 3 to be submitted on development boards. All circuits are required to be constructed using breadboard, stripboard or printed circuit board. The use of development board will not gain credit for circuit construction.

To gain the full range of marks in system development candidates are required to use 8 or more different commands. Using the same command multiple times only counts as one. For example WAIT 10 and WAIT 20 used in the same program will count as one command.

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