GCE AS Examiners' Report

Electronics

AS level

Summer 2024

Introduction

Our Principal examiners' report provides valuable feedback on the recent assessment series. It has been written by our Principal Examiners and Principal Moderators after the completion of marking and moderation, and details how candidates have performed in each component.

This report opens with a summary of candidates' performance, including the assessment objectives/skills/topics/themes being tested, and highlights the characteristics of successful performance and where performance could be improved. It then looks in detail at each unit, pinpointing aspects that proved challenging to some candidates and suggesting some reasons as to why that might be.[1]

The information found in this report provides valuable insight for practitioners to support their teaching and learning activity. We would also encourage practitioners to share this document – in its entirety or in part – with their learners to help with exam preparation, to understand how to avoid pitfalls and to add to their revision toolbox.

Further support

Document	Description	Link
Professional Learning / CPD	Eduqas offers an extensive programme of online and face-to-face Professional Learning events. Access interactive feedback, review example candidate responses, gain practical ideas for the classroom and put questions to our dedicated team by registering for one of our events here.	https://www.eduqas.co.uk/home/professional-learning/
Past papers	Access the bank of past papers for this qualification, including the most recent assessments. Please note that we do not make past papers available on the public website until 12 months after the examination.	Portal by WJEC or on the Eduqas subject page
Grade boundary information	Grade boundaries are the minimum number of marks needed to achieve each grade. For linear specifications, a single grade is awarded for the subject, rather than for each component that contributes towards the overall grade. Grade boundaries are published on results day.	For unitised specifications click here: Results and Grade Boundaries and PRS (eduqas.co.uk)

[1] ***Please note that where overall performance on a question/question part was considered good, with no particular areas to highlight, these questions have not been included in the report.***

Exam Results Analysis	Eduqas provides information to examination centres via the WJEC Portal. This is restricted to centre staff only. Access is granted to centre staff by the Examinations Officer at the centre.	Portal by WJEC
Classroom Resources	Access our extensive range of FREE classroom resources, including blended learning materials, exam walk-throughs and knowledge organisers to support teaching and learning.	https://resources.eduqas.co.uk/
Bank of Professional Learning materials	Access our bank of Professional Learning materials from previous events from our secure website and additional pre-recorded materials available in the public domain.	Portal by WJEC or on the Eduqas subject page.
Become an examiner with WJEC.	We are always looking to recruit new examiners or moderators. These opportunities can provide you with valuable insight into the assessment process, enhance your skill set, increase your understanding of your subject and inform your teaching.	Become an Examiner | Eduqas

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Executive Summary

Candidates' performance in AS Electronics this year, was broadly in line with previous years. The mean mark for Component 1 (exam paper) was slightly higher than 2023; the mean mark for Component 2 (NEA) was slightly lower than 2023. The standard deviation of marks for both components was very similar to previous years.

Analysis of responses to questions showed the level of difficulty of the Component 1 exam to be similar to 2023. It should be noted however that the statistics are based on a relatively small number of entries for this qualification.

Component 1: Principles of Electronics (exam)

This year's paper included questions on every section of the specification. Questions required recall and application of knowledge, with some more demanding questions requiring candidates to evaluate designs or give explanations of circuits.

Most candidates were able to recall the operation of standard circuits and solve numerical problems well. Some candidates were less able to give longer, descriptive answers that were coherent and logically structured. Some candidates scored low marks in the QER questions, and some did not attempt them.

Component 2: System Design and Realisation Tasks (NEA)

NEA work presented by centres was well organised and most was accurately marked. Only a small minority of centres' marks required adjustment by moderators. Most centres' work comprised of a wide range of different projects however for some centres there were several similar projects, addressing the same design brief. The specification requires candidates to select their own focus for the tasks, based on an individually identified problem.

Many candidates produced excellent reports with extensive photographic evidence of the finished circuit as well as stages of testing. In System Planning, many candidates did not provide meaningful design parameters. A full specification should include quantitative, measurable parameters. For the Evaluation, candidates must evaluate the performance of the complete system, comparing measured performance with the design specification. Poor evaluations were often found in reports with few measurable parameters stated in the specification.

Areas for improvement	Classroom resources	Brief description of resource
Quality of response (QER) questions.	AS Electronics eBook	Chapters cover the full content of the specification with worked examples, exercises and practical investigations for each topic.
	Knowledge organisers	Concise summary of each topic, to assist with planning answers to QER questions.
	Past papers and mark schemes	Past papers and mark schemes (available on Portal) contain examples of QER questions and answers.
	CPD material	CPD material on Portal contains commentary from previous series and examples of answers
NEA The specification should give details of an individually chosen problem. System Planning and Evaluation.	AS Electronics specification	Description of the NEA requirements and marking criteria.
	Guidance for Teaching	Further guidance on the NEA with an exemplar project, marked and annotated.
	CPD material	CPD material on Portal contains commentary from previous series and examples of NEA work.

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COMPONENT 1 PRINCIPLES OF ELECTRONICS

Overview of the Component

The Component 1 paper this year had questions from every topic section in the specification. Candidates were given the opportunity to demonstrate their ability to recall and apply their knowledge in a range of familiar and original systems. There were several occasions on which they were tested on their ability to evaluate designs or explain why certain events occurred. From the scripts seen it is apparent that most candidates can recall standard circuits and use equations to solve numerical problems. However, a very significant number struggle when it comes to writing longer, coherent and logically structured answers. There were many complete omissions of the QER questions.

Comments on individual questions/sections

Q.1 **(a)** **(ii)** The supply voltage was often used instead of calculating V_1 first.

(b) To gain the second mark candidates had to explain that the power calculated was greater than the resistor power rating.

(c) Many just calculated the voltage across the equivalent resistor not the residual voltage across the load.

Q.2 **(b)** **(i)** Many candidates had difficulty explaining why a pull-down resistor is needed.

(iii) The emboldened print specifically asked for two 2-input logic gates. Few correct answers were seen with lots of circuits leaving the pulse generator unconnected.

(c) A great number of candidates wrongly used the 2.3V given for the LED rather than calculating the voltage across the current limiting resistor.

Q.3 **(c)** Diagrams of NAND replacement and redundancy were much better than in previous years.

(d) Almost all candidates were able to successfully de Morgan the 3rd term for 1 mark but were unable to simplify the result. Those that could use brackets to eliminate terms got as far as the 3rd mark but did not realise an example of the final simplification was given in the data booklet.

Q.4 **(b)** **(i)** As the result is known in advance candidates must show clearly how to achieve it.
The best method was to find the period, T = 10s.

(ii) The answers must be the simplest terms. Those with multiple terms should have aroused suspicion.

(c) **(ii)** Unfortunately many zero mark answers were seen. The diamond shaped box has to contain a YES/NO question and direction arrows must be shown on the link.

Q.5 **(a)** Disappointingly very few answers scored more than one mark. Candidates just looked at the timing diagrams and drew pulses between the various edges rather than looking back at the circuit diagram and realising that the signal at P is the 10s monostable pulse, triggered by the falling-edge of T.

(b) The question asked <u>why</u> the NOT gate was needed. It was not enough to simply say it inverted the signal. There had to be an explanation in terms of converting a falling edge from the monostable to a rising edge to operate the D-type.

(c) The 555-monostable is a standard circuit but in many responses the capacitor was missing completely.

Q.6 **(b)** Lots of $\sqrt{2}$ were seen in all combinations rather than the simple 12 -1.4V.

(c) Although most candidates gained some credit, this is one area in which they should be encouraged to take more time to draw accurate graphs, of higher quality.

Q.7 **(a)** The QER was poorly answered with many complete omissions. Those who did attempt it often just did one or two calculations without any real evidence of understanding or interpretation of the meaning of the data.

(b) By contrast the Schmitt invertor section was answered extremely well.

Q.8 No areas to highlight.

Q.9 **(b)** There had to be a reference to adjusting the threshold voltage or light activation level not just change the resistance.

(c) The maximum current of 30A was incorrectly used in the formula rather than 6A from the circuit diagram. Where this error was repeated in the power equation ecf was applied.

(d) Candidates found this part very difficult as it required reasoning applied to an unfamiliar situation. This was despite it immediately following a question about the power, which was intended as a hint. Neither of the alternative answers given in the mark scheme were see very often.

Q.10 **(b)** This was a familiar topic asked in a different way. Once again lack of care with diagrams lost candidates marks.

(c) Q <u>remains</u> at logic 1. The underlined word was essential. Most candidates had it changing.

Q.11 There were three aspects to be considered when answering this QER question. These were the voltage gain, bandwidth and slew-rate. There were a lot of complete omissions for this question despite the formulae being available in the data booklet. Those that had a go usually successfully calculated the gain and often correctly identified clipping distortion. A few calculated the bandwidth correctly but most then failed to comment that the frequency range was suitable for this application. Only a handful of candidates were able to calculate the slew-rate correctly and propose the necessary change. Those that suggested a reduction in gain or increase in saturation voltage to address the clipping distortion rarely went on to investigate how these changes might affect the other quantities.

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COMPONENT 2 SYSTEM DESIGN AND REALISATION TASKS

Overview of the Component

This component requires each learner to complete three tasks independently. The tasks build on the concepts studied throughout the specification and the requirement to relate practical circuit design and realisation to knowledge gained from the study of Component 1.

Task 1 (20 marks) – involves the development of a digital system.
Task 2 (20 marks) – involves the development and investigation to test an analogue system.
Task 3 (20 marks) – involves the development of a microcontroller system programmed via flowchart software.

Tasks
Comments on tasks/questions relating to candidate performance/meeting assessment criteria

General Comments

Thanks are extended to centres for their effort in both organising candidates' work for moderation and the online recording of centre marks. The assessment of the work was within tolerance in most centres but in a very small number of centres, adjustments to marks were required. This compared favourably with previous series.

In most centres candidates produced a very good range of projects. In a small number of centres, it appeared that candidates were provided with a common design brief for Task 2. The specification requires candidates to select their own focus for the tasks based on an individually identified problem and this is expected to produce a wide range of tasks within a centre.

In all three tasks:

- In the System Planning section many candidates struggled to provide meaningful parameters and simply quoted power supply values, current consumption and cost without any justification. A full specification should include measurable parameters and numerical data justified by analysis of relevant research of the problem.
- Another common weakness was in the Evaluation section. To gain the full range of marks for the evaluation candidates must make valid, critical and objective evaluation of the performance of the complete system. The evaluation should compare the system with the design specification. A poor evaluation was often the consequence of having few realistic measurable parameters in the specification which then resulted in some simplistic evaluations.
- An important characteristic of a successful report was where candidates made extensive use of screenshots and photographic evidence. Several candidates provided screenshots of simulation results alongside photographs of the corresponding test results on the physical circuit, which displayed voltmeter readings and/or oscilloscope traces. This approach allowed the candidates to easily make comparisons and analysis of their results.

Task 1

Digital tasks should be based mainly on the combinational logic and/or sequential logic systems topics within the specification to access the full range of marks. In a small number of centres all candidates attempted a fairly simplistic design. For example, an astable and a push switch connected to an AND gate. This would not normally provide sufficient scope to allow candidates to access the full range of marks. In contrast candidates in several centres produced outstanding digital tasks which could easily have provided the basis for an A level extended task.

Task 2

Although an improvement was seen compared with previous series, the range of design briefs produced was quite limited. In a number of centres, all candidates attempted almost identical investigations.

Some variation could be achieved within a centre by candidates:

- using different configurations such as inverting/non-inverting/summing op-amps
- using different families of op-amp such as LM741, TL081, CA3140.
- varying the tasks by investigating frequency response, or slew rate, or the effect of both DC and AC signals used with a summing amplifier.

Candidates could also consider investigating the effect of different values of load resistance. and smoothing capacitor on the ripple voltage produced in a rectifier circuit connected to a low voltage AC power supply.

Task 3

Candidates produced a very good range of tasks. Candidates from several centres provided complex design briefs with excellent solutions that included several sub-routines.
It is important that the flowchart diagrams included in the reports are large enough to enable the commands to be read. To gain the full range of marks for system development, simulation tests should be carried out for the flowchart program. Screenshots of the simulation tests should be provided for different combinations of input conditions.
Many candidates failed to provide documentation for simulation tests and were consequently unable make comparisons of the results obtained on the physical circuit.

Task marking
Comments on approaches to internal marking

Annotation on the scripts and mark schemes greatly aids the moderation process. In particular an indication on the mark scheme of which level descriptors were or were not achieved is very helpful. A small number of centres did not provide any annotation or indication on the mark scheme, making accurate feedback to centres very difficult.
It might be useful for centres to look at the approach used for annotation on the marksheets and on the scripts in the Guidance for Teaching on pages 19-41.

Supporting you

Useful contacts and links

Our friendly subject team is on hand to support you between 8.30am and 5.00pm, Monday to Friday.

Tel: 029 2240 4254
Email: electronics@eduqas.co.uk
Qualification webpage: Eduqas A/AS Level Electronics

See other useful contacts here: Useful Contacts | Eduqas

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