GCSE Examiners' Report

Electronics

GCSE

Summer 2026

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Introduction

Our Principal Examiners' report provides valuable feedback on the recent assessment series. It has been written by our Principal Examiners and Principal Moderators after the completion of marking and moderation, and details how candidates have performed in each component.

This report opens with a summary of candidates' performance, including the assessment objectives/skills/topics/themes being tested, and highlights the characteristics of successful performance and where performance could be improved. It then looks in detail at each unit, pinpointing aspects that proved challenging to some candidates and suggesting some reasons as to why that might be.[1]

The information found in this report provides valuable insight for practitioners to support their teaching and learning activity. We would also encourage practitioners to share this document – in its entirety or in part – with their learners to help with exam preparation, to understand how to avoid pitfalls and to add to their revision toolbox.

Further support

Document	Description	Link
Professional Learning / CPD	Eduqas offers an extensive programme of online and face-to-face Professional Learning events. Access interactive feedback, review example candidate responses, gain practical ideas for the classroom and put questions to our dedicated team by registering for one of our events here.	https://www.eduqas.co.uk/home/professional-learning/
Past papers	Access the bank of past papers for this qualification, including the most recent assessments. Please note that we do not make past papers available on the public website until 12 months after the examination.	Portal by WJEC or on the Eduqas subject page
Grade boundary information	Grade boundaries are the minimum number of marks needed to achieve each grade. For unitised specifications grade boundaries are expressed on a Uniform Mark Scale (UMS). UMS grade boundaries remain the same every year as the range of UMS mark percentages allocated to a particular grade does not change. UMS grade boundaries are published at overall subject and component level. For linear specifications, a single grade is awarded for the subject, rather than for each component that contributes towards the overall grade. Grade boundaries are published on results day.	For unitised specifications click here: Results and Grade Boundaries and PRS (eduqas.co.uk)

[1] ***Please note that where overall performance on a question/question part was considered good, with no particular areas to highlight, these questions have not been included in the report.***

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Exam Results Analysis	Eduqas provides information to examination centres via the WJEC Portal. This is restricted to centre staff only. Access is granted to centre staff by the Examinations Officer at the centre.	Portal by WJEC
Classroom Resources	Access our extensive range of FREE classroom resources, including blended learning materials, exam walk-throughs and knowledge organisers to support teaching and learning.	https://resources.eduqas.co.uk/
Bank of Professional Learning materials	Access our bank of Professional Learning materials from previous events from our secure website and additional pre-recorded materials available in the public domain.	Portal by WJEC or on the Eduqas subject page.
Become an examiner with WJEC.	We are always looking to recruit new examiners or moderators. These opportunities can provide you with valuable insight into the assessment process, enhance your skill set, increase your understanding of your subject and inform your teaching.	Become an Examiner | Eduqas

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Executive Summary

Candidates' performance in GCSE Electronics this year was broadly in line with 2025. Following a significant increase in marks last year, the mean marks for both exams were slightly lower than in 2025. The mean mark for the NEA was slightly higher. Analysis showed the level of difficulty of exam questions to be similar to 2025.

Component 1 & 2 exams

The questions in both exams covered all topics in the specification with some synoptic elements, requiring drawing together of knowledge from both components. A wide range of marks were achieved, with some candidates achieving close to full marks. The mean mark in Component 2 was again slightly less than Component 1, reflecting the more demanding topics in Component 2. The majority of questions were attempted. As in previous years, the QER questions were those most often omitted.

In Component 1, candidates performed well in questions on circuit analysis, logic gates, truth tables and resistor colour codes. In Component 2 the highest marks were achieved in questions on flowcharts and the 555 timer.

Candidates scored the fewest marks on both papers, in the QER questions. For each, candidates had to evaluate a circuit to determine whether it met a given specification. Many candidates lacked sufficient understanding of the operation of the circuits to be able to analyse them correctly. There were however examples of excellent QER answers. Candidates also scored low marks in questions on RC timing circuits, half-wave rectification and plotting graphs in Component 1. In Component 2 low marks were achieved in questions on the BCD counter and summing amplifier. Poor quality of presentation was again seen by some candidates, with badly drawn diagrams, rulers not used and multiple crossing out.

The GCSE Electronics eBook includes examples and exercises on all topics. This and other resources are free and available on the GCSE Electronics resources webpage.

Component 3 NEA

For the first time this year, centres were required to submit NEA samples electronically via the IAMIS system. Centres are thanked for preparing well-organised samples and correctly uploading them by the submission deadline. This was helpful in ensuring that online moderation could be carried out effectively.

The Electronics Task Forms were revised this year to add codes, identifying each of the marking criteria. Most centres submitted the revised forms and used the codes to annotate work. Clear annotation on the Task Forms and scripts is very helpful in justifying marks awarded by centres. The revised forms are available on the Electronics webpages under 'NEA'.

Centres are reminded that candidates should choose their own, individual project. This should be discussed with the teacher and the relevant section of the Task Form signed.

Work was accurately marked by most centres, with only a minority of centres' marks requiring adjustment. Examples of high standard projects were seen, with excellent photographic evidence of testing and finished circuits. In some reports images were small or unclear and centres are asked to ensure that images uploaded are clearly visible.

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Component 1 – Discovering Electronics

Overview of the Component

This component is aimed at testing the fundamental concepts of electronics and is broken down into small parts to test multiple factors of candidates' knowledge of the essential topics needed to make progress in the subject.

Candidate performance in this component was good overall with some excellent answers being observed across the whole range of questions.

There were a small minority of candidates who achieved very few marks, as much of their scripts were left blank leaving nothing for examiners to attribute any marks to. In contrast a small number of candidates achieved near full marks. No candidates achieved full marks in the paper.

The question paper was broken down into 44% (AO1), 44% (AO2) and 12% (AO3).

The topics tested were:

1. Basic logic gates / truth tables
2. System design using a functional block approach / operation of a simple RC timing circuit
3. Use of Ohm's Law / circuit voltage / current rules and resistor colour code.
4. Half-wave diode rectifier
5. Regulated power supplies.
6. Component identification by interpreting test results
7. Interpretation of logic circuits to produce Boolean expressions / truth table completion / conversion of logic circuits to NAND gates
8. Transistor switching circuits
9. Sensing circuits using an operational amplifier

There were synoptic elements in questions 2(c) and 9. These required candidates to draw together knowledge from both components.

The overall performance of the paper was good with an overall mean mark of 57.5 for matched candidates which is a slight decrease from 58.1 in 2025. Across all candidates, marks ranged from 2 to 78.

In general candidates attempted the majority of questions. The most successful question was the circuit analysis question (question 3) which had proved in previous years to be quite difficult. The mean mark for this question was 11/13 which shows a continuation of the improvement seen last year. Candidates also performed well in questions involving logic gates, truth tables and resistor colour codes.

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In contrast the QER question was the least successful question on the paper with a significant number of candidates omitting the question completely. The question tested the ability of candidates to analyse and evaluate a circuit design and communicate their understanding in extended prose. Many candidates showed insufficient understanding of the operation of the circuit to evaluate it correctly. However there were examples where candidates gave correct calculations and modifications and achieved good marks.

The quality of presentation in a number of candidates' answers was poor compared to previous years, for example, diagrams drawn in ink instead of pencil with multiple crossing out. No attempt to redraw a messy diagram on the spare pages, made it very difficult to award marks on a few occasions. The use of a ruler was sparse and when it was used some candidates were unable to follow graph paper grids accurately.

There seems to be an increase in the number of candidates using word-processors to prepare the answers. Given that this is their normal way of working they should be able to use an equation editor to lay out mathematical solutions clearly.

Comments on individual questions/sections

1. A successful question for the majority of candidates. A few lost marks in part (a) for failing to identify pin 1 on the diagram. In part (b) some candidates only showed one input to their logic gate symbol, whilst others did not show an output.

2. A number of candidates seemed to be unaware of the function of the given functional blocks. This may be due to the long period of time elapsed since covering the block diagram approach but sorting these into input / processing / output was poor. This lead to further difficulties in constructing a working block diagram to meet the specification. There were far too many examples of complete randomisation of blocks placed into the diagram, for example the temperature sensor and latch were often seen despite there being nothing in the specification that would require their use.

   The synoptic element, 2(c), which required knowledge of the basic resistor-capacitor delay circuit was poorly answered by the majority of candidates. Candidates struggled to draw a capacitor decay curve after the point when the switch was released. Only a handful of candidates were able to identify the weakness of this circuit being that any load connected to the circuit would dramatically change the timing of the delay.

3. Circuit rules for voltage and current are showing some improvement for a number of candidates. Many candidates are still mixing up the relevant units Volts, Amps and Ohms for basic circuit parameters. The resistor colour code was well understood for the majority of candidates.

4. The number of candidates who were unable to identify the diagram for a half-wave rectifier was quite surprising. The facility factor was only 0.65 as candidates were unable to sketch the output of the circuit, lacking the ability to draw just the positive half-cycle and reduce the peak voltage by 0.7 V. This resulted in a low mean mark for the question of 2.6 / 4.

5. Responses showed a lack of understanding of the basic operation of the Zener diode to produce a regulated voltage by a number of candidates. As this is the main source of providing a regulated voltage supply at this level, there are clear misunderstandings about this particular circuit. Candidates found it difficult to determine the current available to the load, often choosing the wrong voltage to use in the formula.

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6. Candidates' graph plotting skills were poor, with very jerky graphs being drawn as a series of straight lines between points rather than a smooth curve. This was generally caused by very inaccurate plotting giving strange looking graphs. Even so despite the curve being of a very unique shape, very few candidates were able to identify the component as a diode.

7. A number of candidates struggled with completing standard Boolean expressions from a logic gate circuit. A number of candidates used the intermediate letters J, K and L in their final expressions instead of A and B as required by the question. In part (b) the Truth Table was usually completed correctly by the majority of candidates. In part (c) several candidates do not know the NAND equivalent circuits for standard logic gates making identification of double inversions impossible.

8. The transistor switch is still not well understood by a large number of candidates. Even though each part of the question took candidates through the route to complete the entire question, candidates failed to select the correct equations in many parts.

9. Candidates found the QER question on a comparator design quite difficult and a number of candidates omitted the question entirely. Evaluating a given circuit is a much higher level skill than that required for other types of questions. It requires in-depth understanding to be able to analyse a circuit correctly and is therefore a very good discriminator to identify the strongest candidates.

   Candidates had to determine if the comparator circuit design provided was suitable, by performing appropriate calculations to identify if the circuit would meet a given specification. Despite two possible routes to work through, it proved to be challenging.

   The interface between the comparator and the MOSFET was part of the solution and it was difficult to assess whether it was the synoptic part of the question that caused a problem or the general issue of not understanding what the circuit was doing. There were however many examples where correct calculations and modifications to the MOSFET driver circuit were detailed by the candidates.

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Component 2 – Application of Electronics

Overview of the Component

This component is aimed at testing the application of electronics in larger systems and requires candidates to apply knowledge about basic building blocks to their function in larger systems.

Candidate performance in this component was lower than that in component 1 reflecting the fact that this paper is based more on application to whole systems rather than straight recall questions. A number of low marks were observed, however there were still a number of excellent answers across the whole range of questions.

The question paper was broken down into 44% (AO1), 44% (AO2) and 12% (AO3).

The topics tested were:
1. 7 segment displays / BCD counting systems
2. Flowcharts as part of larger control system
3. 555 monostable circuits / transistor driver circuit / resistor combinations
4. Non-Inverting amplifiers / inverting amplifiers / clipping distortion / gain-bandwidth product
5. Applications of D-type flip-flops
6. 555 astable circuits / decade counters / logic system design / frequency
7. Summing amplifiers

There were synoptic elements in questions 3 (b)(ii), 3(c), 5(b)(ii) and 6(c)(i). These required candidates to draw together knowledge from both components.

The overall performance in the paper was good with an overall mean mark of 52.7 for matched candidates which is slight decrease of 1.3 from 2025, and 4.8 marks below the mean for Component 1. Traditionally the Component 2 mean has been lower than Component 1 due to the much higher demand of dealing with large systems requiring application of understanding rather than straight recall.

There was a consistent attempt rate at all questions with the exception of the QER question where the attempt rate fell below 90%. Several candidates made no attempt to answer the question at all. Despite this candidates' marks ranged from 0 to 79.

Candidates performed well in questions on flowcharts and the 555 timer. Questions involving the BCD counter and summing amplifier caused most difficulty.

The quality of presentation in some candidates' answers continues to be poor compared to previous years as in Component 1. As mentioned for Component 1, an increase in the use of word processors is being observed yet the need for an equation editor is even more important in this component due to more quite complex formulae.

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Comments on individual questions/sections

1. This question was intended to provide a straightforward introduction to the paper but the facility factor was much lower than expected. Part (a) proved a problem for a number of candidates who were unable to show which segments needed to be on, to produce a particular letter / number or write down the letter / number displayed when given the number of segments lit.

   Part (b) also proved to be poorly answered with candidates unable to give the reason for a debounced switch as to ensure only 1 count is recorded by the counter, for each press of the switch. In part (c) a very large number of candidates continued the binary count instead of resetting after a count of nine.

2. No specific issues to highlight. Candidates found the flowchart based question quite accessible and the majority were able to complete this without too much difficulty.

3. A significant number of candidates were unable to determine the time duration of the pulse in part (a). In part (b)(i) the timing circuit was poorly answered, many omitting the capacitor from the circuit altogether.

   Part (b)(ii) proved to be equally difficult. Candidates found it challenging to correctly add the transistor switch interface to the monostable. The symbol for the transistor was poorly drawn and the motor was often located in the emitter circuit rather than the collector circuit. As there were marks for each part of the interface most candidates achieve 1 or 2 marks out of the 5. A small number of candidates did not attempt any sort of interface circuit and left this part of the diagram blank.

   Candidates did well in part (c). A significant number chose the parallel option of the 12k and 18k resistors rather than the more straightforward solution of 1.1k, 2.2k and 3.9k in series, where only addition was needed.

4. This question was based on non-inverting and inverting amplifiers. A number of candidates could not identify the circuit as a non-inverting amplifier and chose the incorrect formula for part (a). In part (b), reading the graph scale caused issues for some candidates leading to an incorrect output signal value which is not clipped. E.c.f. was applied where possible.

   In part (c) a different amplifier was used which did produce a clipped output. This was missed by a number of candidates. The drawing of the gain-frequency response illustrated a lack of understanding of how the bandwidth was measured with a number of candidates failing to determine the break frequency as 0.7 of the maximum gain. In similar fashion there is a misunderstanding that the gain-frequency product is a constant, so the two parameters are inversely proportional i.e. if one values goes up the other must come down to achieve the same constant.

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5. The basic operation of a D-type in part (a) was demonstrated well by the majority of candidates. Only the weakest candidates failed to score marks on this part.
In (b) the main issues were caused by poor drawing skills - too many candidates using ink instead of pencil and then having to make significant crossing out when realising that a mistake has been made. The vast majority of candidates scored full marks in (b)(ii). Where candidates did make an error it was either to ignore the '0' giving the answer as 82 or taking the literal lookup of Brown as '1', giving the answer as 821. In part (c) a number of candidates found it difficult to explain the action of a latch, neglecting to state that when SW1 is pressed the LED comes on **and stays on** until SW2 is pressed to reset the system.

6. This question combined a 555 monostable with a decade counter and represented a complex system. This caused a lot of candidates difficulty, resulting in a facility factor of just 0.58. In part (a) the usual issues of selecting the incorrect formula and failing to use the correct multipliers resulted in many marks being lost by all bar the strongest candidates. A large number of candidates seemed to miss part (b) as no attempt was made to add the required reset from Q6 to R.

   Part (c)(i) was well done by the majority of candidates, the majority managing to complete the truth table for the dice display correctly. As the specific orientation of the dice was not specified, there were four possible correct solutions, so this would have added to the success as all four possible solutions were observed. In part (c)(ii) there was a lack of understanding that the frequency was so low that the user could simply stop on the number they wanted. Hence candidates were unable to suggest that all that was needed was to change the capacitor (and/or resistors), to increase the frequency so that the numbers changed more quickly. Too many suggested alternative solutions like writing random number generators on programmable devices instead when a simple change would achieve the same result.

7. The QER question based around a summing amplifier caused issues for a number of candidates giving a facility factor of just 0.45. A large number of omissions were observed or just very short answers gaining no credit. Those who attempted the calculations were able to determine a problem with the gain of channel A and recommended an increase in R_1 to 300k. Fewer candidates identified that the input terminals were the wrong way round and that the -15 V reference should be 0 V.

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Component 3 – Extended System Design and Realisation Task

Overview of the Component

The NEA is an integral part of the WJEC Eduqas GCSE in Electronics. This component requires each learner to produce a single extended system design and realisation task independently.
Centres are to be thanked for their effort in uploading candidates' work and entering marks online for the first time this year. This was completed accurately by the majority of centres, by the submission deadline, which was very helpful for online moderation.

Most centres used the correct, revised Electronics Task Forms with codes identifying each of the marking criteria. These forms also contained a focus for each candidate's task, which should be agreed and signed off by the teacher. Centres that did not use these correct forms should use them when submitting future moderation samples. These are available on the Electronics webpages under 'NEA'.

Most centres provided annotation on candidates' scripts showing the evidence for awarding each level descriptor. Centres that did not do so should ensure that work is annotated next year. This is very helpful in justifying marks awarded by the centre during the moderation process.

Most centres provided excellent photographic evidence of the candidates' testing and circuits. In a minority of reports, photographs were too small for details to be legible. Centres are requested to ensure that clear images are provided.

The assessment of the work was accurate for many centres but some centres' marks required adjustment.

Tasks
Comments on tasks/questions relating to candidate performance/meeting assessment criteria

The candidates of most centres produced a very good range of projects. However, in some centres many of the candidates' work seemed to have focused on a common theme. Candidates should focus on their individually identified problem to enable them to write a design specification.

System Planning

Design specifications should contain a range of both qualitative and quantitative terms based on their analysis of the problem. To access the higher band, the specification should contain **detailed measurable electronic parameters**. Examples amongst many acceptable measurable parameters this year included the temperature at which the circuit activates, the time duration for circuits to be active, the required frequency for systems to be random and the number at which a counting system should reset.

Unless candidates provide very good reasons as justification, neither the battery supply voltage nor the current consumption of circuits should be considered as valid quantitative specifications.

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System Development

Many candidates this year showed a high standard of rigorous sub-system testing. These centres set up their sub-systems on breadboard and showed excellent photographic evidence of the test instruments in use. The results were presented in tables and graphs and analysed logically.

Sub-systems should be constructed and tested individually during development of the system rather than testing each sub-system of the fully assembled final circuit retrospectively.

Centres that choose to carry out tests on circuit simulations should note that results are only valid if the actual components such as BC108 or 2N5060 are used rather than generic components such as IC1 and Q1.

Some centres awarded top band marks for development when there were less than five different sub-systems developed. Testing two very similar sub-systems should not be credited as two separate tests. For example two thermistors set to two different temperatures should be considered as one sub-system test but with two sub-sections. A potential divider reference voltage for a comparator should be considered as one sub-system rather than two. Centres should also ensure that marks are not awarded for single component tests. Sub-systems should consist of more than one component.

For each sub-system a test reading should be provided with the output activated and non-activated using appropriate instruments. For example, an oscilloscope would be more appropriate to measure astable and monostable timings than a stopwatch and should be credited accordingly.

When using a flowchart program, simulation tests should be carried out for the program and include screenshots of the results. The flowchart itself should be credited as only one of the five valid tests required to award top band marks.

System Realisation

Centres generally either produced their circuits on breadboard or PCB. If candidates produce the final circuit on PCB, then before and after layout diagrams, showing their modifications to the software generated layouts must be included. Similarly a **clear photo** and a diagram of the plan layout should be included for a breadboard.

As was the case with sub-system testing, many centres this year showed a high standard of final circuit testing using appropriate test equipment and included clear photographic evidence of the actual testing taking place. They demonstrated in depth analysis and comparison of their numerical results with their quantitative specifications.

Some of the testing however, tended to be observational with limited use of test equipment. The recording of test results tended to lack detail and the analysis of the results was superficial. Marks were sometimes awarded for reliable operation of 5 sub-systems when glaring errors could be seen in the circuits. Centres should also ensure that marks are only awarded for the circuit diagram if the diagram matches the final built circuit. As for System Development, circuit diagrams produced by simulator packages should only be considered correct if all components are labelled correctly. Diagrams containing ideal components such as IC1 or Q1 should not be considered fully labelled.

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Evaluation

Good practice evaluations made valid, critical and objective evaluations of performance against measurable numerical electronic design parameters in the specifications. Evaluations should compare measured values obtained during the final full circuit testing against the measurable parameters in the specification. For example, the design specification time for an alarm to sound (with tolerance if applicable) should be compared with the actual value measured in the final physical circuit.

Many centres over awarded marks in this category because the original specification did not have realistic measurable parameters. This resulted in simplistic evaluations.

Many candidates made valid realistic suggestions for improvements. To access the higher band, candidates must explain fully how their suggestions would lead to the improvements.

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Supporting you

Useful contacts and links

Our friendly subject team is on hand to support you between 8.30am and 5.00pm, Monday to Friday.
Tel: **029 2240 4254**
Email: electronics@eduqas.co.uk
Qualification webpage: GCSE Electronics | Eduqas

See other useful contacts here: Useful Contacts | Eduqas

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