GCE AS EXAMINERS' REPORTS

ELECTRONICS
AS

SUMMER 2022

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ELECTRONICS

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COMPONENT 1: PRINCIPLES OF ELECTRONICS

General Comments

The examination proved accessible to most candidates and there were very few omissions of whole questions. The overall attempt rate was 97%. Statistical data showed that question 1 was the most accessible (FF79.9) with question 11 being least accessible (FF30.3). There were many very good responses to all questions. Candidates marks ranged from 2 to 115.

Comments on individual questions/sections

Q.1 (a) Most candidates successfully gave the expected three term Boolean equation although correctly simplified expressions were also given credit. The Karnaugh map had two possible correct solutions $\overline{\mathbf{B}}.\overline{\mathbf{A}} + \mathbf{C}.\overline{\mathbf{A}}$ or $\overline{\mathbf{A}}.(\overline{\mathbf{B}} + \mathbf{C})$ and this proved very straightforward. The answer to part (iii) similarly had two solutions provided the instruction to use only NOT, AND or OR gates was followed.

(b) The multiplexer was well answered.

(c) A few single input NAND gates were seen but only penalised once. There was an occasional extra NAND gate added to the end of the system, creating NOR instead of OR. Most candidates were able to successfully cross out the two redundant gates.

Q.2 (a) (i) Candidates were expected to use t=RCxln2 to calculate the half-life. A significant number used the full equation with more opportunities for errors to be introduced. Either way the majority got the correct answer.

(ii) The question clearly stated that the capacitor was initially discharged giving a strong hint to which equation was needed. Weaker candidates tended to plump for the first one in the list and hence arrived at 3V instead of 9V.

(iii) Surprisingly a lot of incorrect answer were seen. Despite the word estimate, and the single mark offered, lots of complex calculations were attempted with poor outcomes. This had a knock-on effect for the next part. Use of 5RC or 6RC was expected.

(b) (i) Capacitor graphs shapes should be familiar, so it was surprising to see a lot of poorly draw graphs, with weird shapes. This was usually a result of the incorrect answer to (a) (iii). Instead of re-visited the previous answer many ploughed ahead, even when the time to 12V was estimated to be less that time to reach 9V. Some error carried forward marks were awarded.

(ii) The answer from the candidate's graph was accepted.

(c) (i) Half C instead of 2C was frequently seen.

(ii) Similarly, the time to 7.5V was often halved instead of doubled.

Q.3 The majority gained the mark for the conversion of decimal to binary but only a small number knew how to convert to hexadecimal.

(b) Most candidates found the explanation of the flow chart very straightforward. But as this was a QER question candidates were expected to do more than just copy out the list of instructions. Some linking statements to the application of this flowchart to the brief was expected to gain higher tier marks.

(c) (i) Candidate's answers had to refer to 'avoiding damage to the MOSFET', not the circuit, components or solenoid.

(ii)&(iii) Both parts well answered by most. Occasionally errors for forgetting to square the current or using 8A (24/3) instead of 3A were seen. Rounding to 1.6 lost the last mark.

Q.4 (a) Many candidates drew the more familiar up-counter circuit.

(b) Similarly, the answer offered for this part was frequently the up-counter logic.

(c) (i) Several correct answers were possible as the type of gates to use was not specified. On this occasion marks were awarded for error carried forward from the table.

(ii) This standard calculation of LED current was usually done correctly. The mistaken use of 2.1V or 5V was seen on some occasions.

Q.5 (a) A simple select and use of formula question meant that many got the value of V_{OUT} correct although some omitted the sign and lost a mark. Interim marks were awarded for each correct term in the equation.

(b) This was an application of the inverting amplifier seen in the AS exam before. Any answer that made it clear that the purpose of the subsystem was to invert the previous output voltage was allowed.

(c) As the application of the summing amplifier has proved challenging in the past part (i) was introduced to give an extra hint. A very commonly seen answer was 7.2V, arising from candidates ignoring the text and graphs of part (c) and using the formula from part (a) with V_Q set to 0V. Unfortunately, many who did gained the amplitude mark did not apply it to part (ii) and used a completely different amplitude, usually 12V. A reasonable number spotted the inversion but only the top scoring candidates gave the off-set effect correctly.

Q.6 (a) (i) Mostly correct answers seen. Candidates should use capital letters for logic gates as on some scripts nor and not were indistinguishable.

(ii) Output T very straightforward and almost always correct. Output Q was rather more challenging due to the number of bars. Although it could be simplified, it was better not to try.

(b) The final mark for C being the redundant gate had to be supported by evidence. When it resulted from incorrect reasoning the mark was not awarded. As in previous years candidates often apply de Morgan's theorem correctly but come unstuck during the simplification of the Boolean. In this case they would score 2 of the marks. The two most common errors were. The omission of the bracket on the (C + A) term or getting 4 two-letter terms instead of 2 three-letter terms when multiplying out the brackets.

Q.7 The majority of candidates approached answering this QER question in a sensible way. They took each of the specification statements and addressed them in turn. The mark space ratio was usually the most successfully dealt with, either using the formulae for mark time and space time separately, or the ratio equation given in the data booklet. It was found to be correct. Calculating the frequency correctly proved more problematic for a good number although most concluded that it was incorrect. Those that established that it was a factor of ten out usually concluded increasing C was the simplest solution. Some very good scripts offered the alternative answer of changing both resistors and thus maintaining the m/s ratio. Working for these answers should always be included.

The final specification point is where most credit was lost. There were two issues to comment on. Firstly, the LED has to be reconfigured by connecting it between the 555 output and 0V (not turning it around as a number of candidates suggested). The second point is that the time ON is only met if the frequency has been correctly altered.

When awarding marks consideration was given to the quality of the response in terms of coherent and logical presentation, as well as spelling, punctuation and grammar.

Q.8 (a) A reference to changes to both input and output was required.

(b) Unless the candidate understands that the whole point of a transition gate is to produce a very short pulse then they tend to only access the first two marks. It is still quite common to see a sequence of graphs with a rising-edge shifting along the time access.

(c) These marks rather depend on the answer to part b. The question specifically asks about changes to signal Q. The pulse width is reduced by 20ns but the pulse start time remains the same.

Q.9 Several parts of this question relate to theory which is well covered in the notes that accompany the course. Very few candidates remembered these accurately enough for full marks but there were opportunities for partial credit.

(a) Some reference to controlling/reducing the gain gained a mark.

(b) Only a handful of scripts showed understanding of virtual earth.

(c) (i) Many scored the mark for gain of 72 but very few referred to the range from 0 to 72.

(ii) These three marks should have been easy to AS level candidates, but a surprising number did not show the signal clipped at 17V, presumably as they did not look back to the start of the question.

(d)(i) A lot of positive feedback drawn and/or resistors in various positions shown.

(ii)&(iii) It was strange to see a wide range of the random numbers suggested here. Knowledge of voltage followers would have provided the answers.

Q.10 (a) (i) A standard Thevenin's theorem calculation with the slight variation of one of the resistances being a thermistor. Generally well-answered by the majority.

(ii) The equivalent circuit needed to be labelled with the values of V_{OC} and R_{EQ} calculated above.

(b) There were several approaches to answering this part. Method 1 calculates the load current by first taking the voltage drop across R_{EQ} and dividing by the value of R_{EQ}. The value of 27mA is significantly less than the 50mA required. Method 2 takes the desired load current of 50mA, calculates the voltage drop across the equivalent resistor and finds the residual load voltage of 4.5V is less than the 6V required for the alarm. Some students calculated the resistance of the alarm and then used a voltage divider approach. All answers had to draw the conclusion that the alarm would not work as specified to gain the full range of marks.

(c) (i) Candidates were expected to start with the h_{FE} formula and carry out the standard transistor calculations. A significant number forgot the final stage of adding 0.7 to the voltage across the base resistor. A fairly common mistake was to use the voltage divider to calculate V_T.

(ii) This was a difficult question as it could be approached in different ways. It was not attempted by many candidates.
However, the first 2 marks were based on a straightforward voltage divider calculation and so should have been readily accessible to most candidates. The remaining three marks required either a Thevenin's theorem approach or analysis of the voltage divider, considering the effect of the load on the voltage. The conclusion that the system would work needed to be stated to get the final mark. Some answers failed to consider the reduced supply voltage of 6V.

Q.11 (a) (i) This was simply a question of subtracting the voltage drop across two diodes from V_S. Lots of answer incorrectly tried to use $\sqrt{2}$ either to multiply or divide the 12V supply.

(ii) The output voltage graphs needed to use the voltage calculated in (i), the full-wave rectification effect and show a small ripple. Few were seen completely correct.

(b) Error carried forward meant that the candidate only had to make the ripple larger than that drawn in (ii). Very few good diagrams were seen.

(c) Candidates were expected to rearrange the ripple formula supplied in the data booklet and substitute in the correct values to find the current. One mark was lost if 50Hz was used instead of 100Hz.

(d) This was also a standard calculation question, based on the zener diode regulator. Common errors were the use of 8.2V instead of 3.8V to calculate the current and either forgetting to deduct 10mA for the zener holding current or adding it.

Summary of key points

- For QER questions the candidate's answers should be in the form of a structured, coherent report with correct punctuation and grammar. Diagrams can be used, where appropriate, but the report needs to be more than just a bullet point list. Where calculations are needed the equations chosen and all the working steps should be shown, and the answer given with appropriate units. In this exam Question 7 is a good example.

- For a good number of questions part of the answer involves standard sub-systems. Candidates should become familiar with these and be able carry out appropriate calculations. Examples include the MOSFET, an LED output, op-amp voltage amplifiers, transistor switches and zener voltage regulators.

- Evaluation skills are tested, these are signalled by key words such as analyse, design and evaluate.

- When simplifying Boolean expressions many candidates ignore the brackets. These are critical and failure to take them into account usually results in most of the marks for that question being lost.

- Candidates need to take greater care drawing diagrams.

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COMPONENT 2: SYSTEM DESIGN AND REALISATION TASKS - NEA

General Comments

Thanks are extended to centres for their effort in both organising candidates' work for moderation and the online recording of centre marks. The assessment of the work was within tolerance in the vast majority of centres but in a small number of centres adjustments to marks were required.

In the majority of centres candidates produced a very good range of projects. In a small number of centres it appeared that candidates were provided with a common design brief from which they developed their own set of parameters. The specification requires candidates to select their own focus for the tasks based on an individually identified problem and this is expected to produce a wide range of tasks within a centre.

The majority of centres provided excellent photographic evidence, but annotation of candidate's work was quite limited. A large number of centres failed to provide any annotation. Annotation on the scripts along with an indication on the task form of which level descriptors were or were not achieved greatly aid the moderation process.

In all three tasks the main weakness was in the System Planning and Evaluation sections.

Many candidates struggled to provide meaningful parameters and simply quoted power supply values, current consumption or simply a list of components. A list of components to be used is not part of a specification. The choice of a particular component may be part of the design solution to a problem but not part of the specification. A full specification should include measurable parameters and numerical data.

A significant number of candidates provided extensive test results but there was very little evidence of analysis of these results.

To gain the full range of marks for the evaluation candidates must make valid critical and objective evaluation of performance. The evaluation should compare the system against the design specification and make suggestions for improvement to access the full range of marks.

The suggestions for improvement must be relevant. The consequence of not having many measurable parameters in the specifications resulted in some simplistic evaluations.

Comments on individual questions/sections

Task 1

Digital tasks should be based mainly from the logic and/or sequential logic systems topics within the specification to access the full range of marks. In a small number of centres all candidates attempted a fairly simplistic design. For example an astable and a push switch connected to an AND gate. This would not normally provide sufficient scope to allow candidates to access the full range of marks

In contrast candidates in several centres produced outstanding digital tasks which could easily have provided the basis for an A level extended task.

The accounts provided for the sub-system testing tended to be observational with very little recording of the testing that took place. For each sub-system a test reading should be provided with the output activated and non-activated.

Task 2

Analogue systems should contain both an analogue input and an analogue output. In a small number of centres all candidates attempted a task based on a light/temperature sensing sub-system connected to a comparator or transistor with a LED output.

To access the full range of marks for system realisation the use of an oscilloscope would normally be required for testing an analogue system.

The focus provided for an amplifier based tasked was an improvement on previous year with a number of candidates providing an investigation of both gain and the frequency response of an amplifier. Some candidates investigated both the DC and AC slew rate for different families of op-amps

Task 3

Candidates produced a very good range of tasks.

For the microcontroller task at AS level, candidates are required to program the microcontroller via a flowchart program; other programming languages are not acceptable. It is important that the flowchart diagrams included in the reports are large enough to enable the commands to be read.

To gain the full range of marks for system development, simulation tests should be carried out for the flowchart program. Screenshots of the simulation tests should be provided for different combinations of input conditions.

Summary of key points

- Candidates' tasks should focus on a problem of their choosing to analyse. A good analysis should enable them to write a design specification, including measurable parameters and numerical data.

- Evaluation must make valid, critical and objective evaluation of performance against the design specification.

- Digital tasks should be based mainly from the logic and/or sequential logic systems topics within the specification.

- Analogue tasks should contain both an analogue input and an analogue output.

- Microcontroller tasks, requires candidates to program the microcontroller via a flowchart program, simulate the program and the download for final testing.

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