GCE A Level Examiners' Report

Subject: Electronics

Level: GCE A Level

Summer 2024

Introduction

Our Principal examiners' report provides valuable feedback on the recent assessment series. It has been written by our Principal Examiners and Principal Moderators after the completion of marking and moderation, and details how candidates have performed in each component.

This report opens with a summary of candidates' performance, including the assessment objectives/skills/topics/themes being tested, and highlights the characteristics of successful performance and where performance could be improved. It then looks in detail at each unit, pinpointing aspects that proved challenging to some candidates and suggesting some reasons as to why that might be.[1]

The information found in this report provides valuable insight for practitioners to support their teaching and learning activity. We would also encourage practitioners to share this document – in its entirety or in part – with their learners to help with exam preparation, to understand how to avoid pitfalls and to add to their revision toolbox.

Further support

Document	Description	Link
Professional Learning / CPD	Eduqas offers an extensive programme of online and face-to-face Professional Learning events. Access interactive feedback, review example candidate responses, gain practical ideas for the classroom and put questions to our dedicated team by registering for one of our events here.	https://www.eduqas.co.uk/home/professional-learning/
Past papers	Access the bank of past papers for this qualification, including the most recent assessments. Please note that we do not make past papers available on the public website until 12 months after the examination.	Portal by WJEC or on the Eduqas subject page
Grade boundary information	Grade boundaries are the minimum number of marks needed to achieve each grade. For linear specifications, a single grade is awarded for the subject, rather than for each component that contributes towards the overall grade. Grade boundaries are published on results day.	For unitised specifications click here: Results and Grade Boundaries and PRS (eduqas.co.uk)

[1] ***Please note that where overall performance on a question/question part was considered good, with no particular areas to highlight, these questions have not been included in the report.***

Exam Results Analysis	Eduqas provides information to examination centres via the WJEC Portal. This is restricted to centre staff only. Access is granted to centre staff by the Examinations Officer at the centre.	Portal by WJEC
Classroom Resources	Access our extensive range of FREE classroom resources, including blended learning materials, exam walk-throughs and knowledge organisers to support teaching and learning.	https://resources.eduqas.co.uk/
Bank of Professional Learning materials	Access our bank of Professional Learning materials from previous events from our secure website and additional pre-recorded materials available in the public domain.	Portal by WJEC or on the Eduqas subject page.
Become an examiner with WJEC.	We are always looking to recruit new examiners or moderators. These opportunities can provide you with valuable insight into the assessment process, enhance your skill set, increase your understanding of your subject and inform your teaching.	Become an Examiner | Eduqas

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Executive Summary

Candidates' performance in A level Electronics this year, was broadly in line with previous years. The mean mark for Component 1 (exam) was very similar to 2023; the mean mark for Component 2 (exam) was slightly lower than 2023. The mean mark for Component 3 (NEA) was similar to 2023. The standard deviation of marks for Component 1 was slightly more than 2023 while the standard deviation of marks for Components 2 and 3 was slightly less.

Analysis of responses to questions showed the Component 1 exam to be of a similar level of difficulty to 2023. Candidates found the Component 2 exam more difficult.

Component 1: Principles of Electronics (exam)
The exam contained questions from all topics of Component 1 and some synoptic elements. Questions required knowledge recall, application, design and evaluation. There were many excellent responses to questions across all topics. Questions on combinational logic were generally answered well, with mixed responses to questions on other topics, requiring application and algebraic manipulation. Some written explanations were minimal and poorly structured.

Component 2: Application of Electronics (exam)
The standard of answers was generally high however questions requiring candidates to give written descriptions or explanations, such as QER, were often poorly answered. In calculations some candidates lost marks when they did not show intermediate steps leading to answers.

Component 3: System Design and Realisation Tasks (NEA)
Centres presented work well and recorded marks accurately. It is helpful when centres show marks awarded on the mark list and annotate work to show where marks have been achieved. Work was accurately assessed by most centres. Adjustments to marks were required for only a small number of centres.

Some excellent reports were seen, scoring high marks in all four sections, with excellent photographic evidence provided. Marks were often lost in the System Planning and Evaluation sections. The design specification should give measurable parameters and numerical data. Candidates must make a valid, critical and objective evaluation of the performance of the system, making comparison with the specification. Suggested improvements must be relevant and state why the improvement would be beneficial.

Areas for improvement	Classroom resources	Brief description of resource
Descriptions and explanations. Quality of response (QER) questions.	A level Electronics eBook	Chapters cover the full content of the specification with worked examples, exercises and practical investigations for each topic.
	Knowledge organisers	Concise summary of each topic, to assist with planning answers to QER questions.
	Past papers and mark schemes	Past papers and mark schemes (available on Portal) contain examples of QER questions and answers.
	CPD material	CPD material on Portal contains commentary from previous series and examples of answers.
NEA – System Planning and Evaluation sections.	A level Electronics specification	Description of the NEA requirements and marking criteria.
	Guidance for Teaching	Further guidance on the NEA with an exemplar project, marked and annotated.
	CPD material	CPD material on Portal contains commentary from previous series and examples of work.

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COMPONENT 1: PRINCIPLES OF ELECTRONICS

Overview of the Component

This exam contained content from all topics of Component 1 along with elements of the core concepts and some synoptic elements in questions 4, 6 and 11. Questions contained a balance of recall, application of knowledge, design, and evaluation. There was also a balance of written explanation and mathematically based responses which was in line with previous years.

Whilst many candidates produced excellent responses in questions on all topics some candidates demonstrated strength in some topics only. As usual the Combinational logic questions such as questions 1 and 2 were particularly well answered with the highest facility factors. The questions that required application of knowledge demonstrated that whilst many candidates were well versed in this some were thrown by a different application from that which they were familiar. In questions where a mathematical response required the use of algebraic manipulation there was a range in quality of responses with some accurate and excellently laid out and others where candidates were unable to carry out the necessary manipulation. Written explanations again displayed a range of quality in responses from clear and well-structured to minimal and poorly structured. Some candidates were unable to identify the key information asked for by the question and thus their response whilst possibly accurate was worth no marks.

Analysis of facility factors of questions showed the paper overall was similar in difficulty to 2023. The mean mark for all candidates was 86.6 (of max mark 140). This is the same as 2023 and slightly higher than the mean mark for 2019 (pre-pandemic).

Comments on individual questions/sections

Q.1 & Q.2 These questions covered many aspects of Combinational Logic and the facility factors for these topics were high as always. The best responses contained logic circuit diagrams that were clear and well-drawn.

Q.3 (a) (ii) Some candidates drew what could have been a correct circuit however the connections to the inputs of the op-amp were unclear due to lines crossing and so full marks could not be awarded. Candidates should use a ‘blob’ to indicate wire connections or a half loop to indicate wires crossing with no connection.

Q.4 This question contained synoptic material for which there were many excellent responses. Some candidates were unfamiliar with the circuit diagrams required which is basic knowledge recall. Candidates should be reminded that they could be required to recall knowledge from all parts of the course.

Q.5 This question had a low facility factor. However, the calculation for part (a) is standard for transistors and whilst there were some perfect responses many candidates found this difficult. Part (c) clearly differentiated those who understood the circuit from those who didn't, and some were unable to provide a coherent or meaningful explanation.

Q.6 & Q.7 Candidates coped well with the drawing together of content across different topics.6(a)(i) Some candidates were unable to identify the logic level from the phototransistor indicating a lack of familiarity of this component. This didn't lead to any difficulties later in the question. However the question demonstrates how candidates should be encouraged to attempt all parts of a question as latter parts were independent of earlier parts.

Q.8 The large standard deviation for this question demonstrates the large range in quality of candidate responses. Many candidates were unable to draw correct graphs in parts (b)(i) and (ii). In part (c) there were a significant number of candidates who were able to carry out these standard calculations on FM however many candidates were unable to select the appropriate data for the equations.

Q.9 Nothing to highlight.

Q.10 There was a low facility factor for this question and also a large standard deviation reflecting the large range in the quality of responses. Whilst part (a) confused some candidates there were some accurate answers with clear working indicating the candidates' route to that answer. There were two methods to approach part (b). Many candidates substituted the voltages into the formula provided in part (a). Others used the summing amplifier formula with their resistor values which allowed ecf for incorrect answers to part (a). Question (c)(i) required an understanding of the relationship between the summing amplifier and the DAC which challenged many candidates.

Q.11 Nothing to highlight.

Q.12 This question included the QER response. As in other parts of the paper there were some excellent responses, very worthy of the full 6 marks. The best responses not only identified the circuit but explained, with calculations, how they reached their conclusion. There were fewer candidates who were put off the extended written response which is encouraging.

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COMPONENT 2: APPLICATION OF ELECTRONICS

Overview of the Component

In general, the standard of answers was high.

Questions 3, 8 and 9 had an appreciable number of marks focussed on the assessment of assessment objective (AO1). In the latter two questions, candidates were required to explain aspects of the topics, such as the effect of interference on PPM and PAM and the way parallel-to-serial conversion is achieved in a shift register. These explanations tended to be weaker than other aspects such as sections involving calculations.

Questions 1 (sequence generator), 4 (optical fibre communications) and 9 (mains power supply), included sections requiring candidates to apply the information provided - assessment objective 2 (AO2). On the whole, the performance was better than that seen for AO1.

Assessment objective 3 (AO3) was addressed largely by circuit design and evaluation in questions 5, 6 and 11 (the QER question). The general performance here was disappointing, particularly on what are standard circuits such as the pre-amplifier in question 6 and the active filter in question 5. A minority of candidates made very little or no attempt to answer the QER task on evaluating the performance of an astable sub-system, suggesting that some may not have practised these skills sufficiently.

It is essential that candidates read the question carefully, take note of the information provided and recognise clues, such as the number of marks provided, and the verb used in it. ‘Explain’ ‘describe’ and ‘state,’ for example, hint at the kind of answer expected.

In questions involving calculations, candidates should be encouraged to show the intermediate steps that lead to the answer in order to receive marks even when the answer is incorrect. A wrong answer, unsubstantiated, earns nothing.

Comments on individual questions/sections

Q.1 In part (a)(iii), completing the table was easier when candidates followed the recommended route of transferring the ‘Next outputs’ to the following line of the table as ‘Current outputs’. Others tended to lose track of the relationship between the state diagram and the table.

Part (b) highlighted the confusion between unused states (states that will eventually lead into the main sequence) and stuck states (states that will never lead to the main sequence.)

In (c), parts (i) and (ii) were usually answered correctly. Part (iii) exposed confusion between NOR, OR, EX-OR and EX-NOR gates.

Q.2 This was well-answered on the whole. As elsewhere in the paper, some explanations to parts (a), (b) and (f) were 'woolly' and muddled. Many answers to part (f) failed to mention the status register and the role of the zero flag.

Q.3 In part (c), many graphs were accurately drawn, showing the 3V drop across the MOSFETs, the clipping as the signal polarity reversed and the bi-directional conduction. However, in (ii), many confused crossover distortion with clipping distortion. The common error in part (iv) was the use of 24V for V_S instead of 48V.

Q.4 In (a)(i), many thought that the signal would travel faster in an optical fibre, ("...at the speed of light...) whereas, in reality, it would be slower because of the refractive index of the glass, compared to microwaves travelling in free space. The power calculation in (ii) and the TDM calculation in part (b) were often correct.

Q.5 Part (a)(ii) asked for an estimate of the output voltage, rather than a calculation. Candidates should have realised that the reactance of the capacitor at 100Hz is so huge compared with the resistance of the resistor, so V_{OUT}, the voltage across the resistor, would be virtually zero.

In part (c) a surprising number of candidates did not know the circuit diagram for an active treble cut filter. They often picked up intermediate marks for having the correct voltage gain and break frequency. In part (ii) many presumably did not have a protractor and lost marks for an incorrect roll-off angle.

Q.6 In answering part (a)(i), candidates were expected to know that the pre-amplifier required a non-inverting amplifier circuit. Many did not. They were required to show by calculation that the bandwidth of the resulting amplifier met the requirement given in the specification.

In (a)(ii), many answers were too vague to be awarded marks. They often failed to mention the significance of the relatively low output impedance of the previous stage.

Q.7 No areas to highlight.

Q.8 Some candidates lost marks in part (a)(i) because of lack of care in drawing the graph. Usually, it was unclear whether or not the amplitude of the PPM pulses remained constant.

In (a)(ii), candidates should have been guided by the mark allocation into suspecting that answers should have referred to two features. Some failed to make it clear that interference affected signal amplitude and that, as a result, PPM pulses which encode data in the timing of the pulses were relatively immune, whereas PAM pulses encode data as pulse amplitude and so were more likely to be affected.

In part (b)(i), a surprising number of candidates failed to convert the binary number correctly, particularly into hexadecimal. In (ii), some missed the significance of the 'Load' pulse, while others failed to observe 'rising-edge' triggering. As in part (a)(ii), candidates should have structured their answers to detail firstly the parallel loading and secondly the serial transfer. Most answers were unclear.

Q.9 The instruction in part (a) said “Complete...”. Many candidates added a full-wave rectifier. In (b)(iii), completely correct answers pointed out that the power dissipated remained constant because both the voltage across the resistor AND the current through it remained constant. Answers to (b)(iii) and (d)(i) were often vague and poorly structured, often hinting at but not ‘nailing’ the full answer. Some candidates could not draw the circuit symbol for a transistor, required in (d)(ii).

Q.10 Parts (a), (b) and (c) - no areas to highlight.
In part (d)(i), it was not enough to identify that switch S3 had been pressed. There needed to be an indication that this was momentary, or equivalent. In part (d)(ii), a full answer contained all four elements shown in the Mark Scheme.

Q.11 The QER question produced answers having a wide range of validity and structure. The best showed a logical and systematic approach. Most covered a range of aspects and made sensible comments on the suitability of the design.

The important factors are outlined in the Mark Scheme.
Most worked out the astable frequency and mark: space ratio. Some judged, harshly, that the astable frequency of 1.02Hz did not meet the specification’s ‘...about 1Hz.’ Common mistakes were to misuse the information about the current demanded by the 555 IC, adding it to the output current and to ignore the effect of the mark: space ratio on the output current. Only rarely did a candidate evaluate the suitability of the battery capacity.

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COMPONENT 3: EXTENDED SYSTEM DESIGN AND REALISATION TASKS (NEA)

Overview of the Component

This component requires each learner to complete two tasks independently. The tasks build on the concepts studied throughout the specification and the requirements to relate practical circuit design and realisation to knowledge and understanding gained from the study of components 1 and 2.

Task 1 (20 marks) – involves the development of a microcontroller system programmed through assembler language.

Task 2 (50 marks) – is a substantial system development, including analogue and digital sub-systems in an integrated design.

Each task enables learners to carry out a design and realisation task based on an individually identified problem, context or opportunity.

Centres are to be congratulated for their effort in presenting candidates' work for moderation, including the online recording of centre marks.

A number of centres showed little indication on the marklist as to why marks were allocated, and some did not show marks at the end of each section. It is good practice to indicate where (and possibly why) marks have been given and also reference it on the candidates' work. The assessment of the work was within tolerance in the vast majority of centres but in a small number of centres, adjustments to marks were required.

Candidates should focus on a problem to analyse that will enable them to write a design specification based on a specific identified problem. Many candidates struggled to provide meaningful parameters and simply quoted power supply values, current consumption and cost without any justification. A full specification should include measurable parameters and numerical data justified by relevant research. Some research was trivial and concentrated on components rather than the requirements of the problem to inform the specifications. Candidates in the majority of centres provided excellent photographic evidence.

As in previous years, a number of candidates had ideal rather than real components in their circuit diagrams. Real components not only model real circuit behaviour but provide an accurate high quality and fully labelled circuit diagram.

A common weakness in both tasks was still in the Evaluation section. To gain the full range of marks for the evaluation, candidates must make a valid, critical and objective evaluation of the performance of the complete system. The evaluation should compare the system performance with the design specification. A poor evaluation was often the consequence of having few measurable parameters in the specifications which then resulted in some simplistic evaluations. Suggestions for improvement must be relevant and should state why incorporating such an improvement would be beneficial rather than simply mentioning better coding, better light sensors or lower tolerance resistors.

Tasks
Comments on tasks/questions relating to candidate performance/meeting assessment criteria

Task 1
For the microcontroller task at A level, candidates are required to program a microcontroller using assembly language, other programming languages are not acceptable.

It was again pleasing to see that no centres allowed candidates to produce hybrid programs that included both assembler and Basic commands (be aware: this is possible within PICAXE but not within the MPLAB environment). However, some candidates generated their code from a flowcharting program. This is unacceptable; candidates should write their own assembler code.

A few centres submitted microcontroller projects containing light sequences which resulted in all candidates within the centre producing very similar programs. As the tasks are from individual problems identified by the candidates, it would be expected that specification parameters would usually be different, and programs would have variations in structure and commands used.

Credit cannot be awarded for commands used to configure the ports. However, credit can be given should these same commands be used by the candidate in their main program and any sub-routine they write. It is good practice to list the commands used.

A few centres did not use the 'Assembly Language Template' provided on the Eduqas website. It is important that centres use this template. All standard sub-routines are listed in it and any sub-routines called and equate statements used should be included in the Task 1 template. It is important that candidates realise that these sub-routines and equate statements actually exist. If centres are using their own template, then this must be submitted together with the candidates' work.

Task 2
A project should consist of block diagram showing a number of sub-systems that are then individually tested and then interconnected and have signals that are transferred from one sub-system to another, as a complete system. How this occurs in terms of the function of each block needs to be explained in the 'Evaluation' section. Development of the complete system from sub-systems must be shown. It is not acceptable to present a complete circuit then cut it up into parts.

Design specifications should contain a range of both qualitative and quantitative terms based on analysis of the problem and contain detailed realistic and measurable electronic parameters. The specifications need to be justified, e.g. if a system is to be used in a car, the power supply is probably 12V, although this can be converted to another value using the necessary sub-system. Sub-system specifications should at the very least give input and output voltages.

Alternative subsystems tended to be simply mentioned in the text in many cases. Also thought needs to be given to their relevance. At the very least, a circuit diagram needs to be included with some predictions of behaviour and reasons given for choice of subsystem. The better candidates also investigated the circuit behaviour of the alternatives.

Again this year, a common misconception was to identify sub-systems and/or components as part of the specification. The choice of a particular sub-system/component may be part of the design solution to a problem but would not normally be part of the specification.

Most candidates provided extensive photographic evidence also showing voltmeter readings at various stages of system development. Although this is useful, it should be considered as a supplement to tabulated results rather than an alternative. Often, even tabulated test results had very little analysis of the results thus leading to a poor evaluation.

The physical circuit layout produced by most candidates was of a very good standard, with the majority of circuits constructed very neatly on breadboard with horizontal and vertical wires not covering ICs or other components.

Task marking
Comments on approaches to internal marking

Annotation of candidates' work, and mark schemes was a great help in moderation however it was limited to only a few centres. A large number of centres failed to provide any annotation on either task. At the very least, an indication on the mark scheme of which level descriptors were or were not achieved, together with marks awarded, would greatly aid the moderation process.

Candidates should focus on a problem that enables them to research and write a design specification based on the specific identified problem. Candidates should select their own focus for the tasks, based on different problems and this is expected to produce a wide range of tasks within a centre.

The range of tasks produced within centres was variable. In many centres, candidates produced a very good range of tasks with some of the work being outstanding and demonstrating considerable innovation. In a very small number of centres all candidates produced similar projects.

Supporting you

Useful contacts and links

Our friendly subject team is on hand to support you between 8.30am and 5.00pm, Monday to Friday.
Tel: 029 2240 4254
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Qualification webpage: Eduqas A/AS Level Electronics

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