GCE AS

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WJEC Eduqas GCE AS in

ELECTRONICS

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SAMPLE ASSESSMENT MATERIALS

Teaching from 2017
For award from 2018

wjec
cbac

For teaching from 2017
For award from 2018

GCE AS ELECTRONICS

SAMPLE ASSESSMENT MATERIALS

Contents

WJEC Eduqas AS in Electronics

Data booklet

A clean copy of this booklet should be issued to candidates for their use during each AS in Electronics examination.

Centres are asked to issue this booklet to candidates at the start of the AS in Electronics course to enable them to become familiar with its contents and layout.

Preferred values for resistors

The figures shown below and their decade multiples and sub-multiples are the E24 series of preferred values.

10, 11, 12, 13, 15, 16, 18, 20, 22, 24, 27, 30, 33, 36, 39, 43, 47, 51, 56, 62, 68, 75, 82, 91.

Standard multipliers

Prefix	Multiplier
T	$\times 10^{12}$
G	$\times 10^{9}$
M	$\times 10^{6}$
k	$\times 10^{3}$

Prefix	Multiplier
m	$\times 10^{-3}$
μ	$\times 10^{-6}$
n	$\times 10^{-9}$
p	$\times 10^{-12}$

Useful equations

$$C = \frac{Q}{V}$$

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$C = \frac{C_1 C_2}{C_1 + C_2}$$

$$C = C_1 + C_2$$

$$V_{rms} = \frac{V_0}{\sqrt{2}}$$

$$I_{rms} = \frac{I_0}{\sqrt{2}}$$

$$I_C = h_{FE} I_B$$

$$I_D = g_M (V_{GS} - 3)$$

$$P = I_D^2 r_{DSon}$$

$$A + \overline{A} \,.\, B = A + B$$

$$A \,.\, B + A = A \,.\, (B + 1) = A$$

$$G = \frac{V_{OUT}}{V_{IN}}$$

$$G = 1 + \frac{R_F}{R_1}$$

$$G = -\frac{R_F}{R_{IN}}$$

$$V_{OUT} = -R_F \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + ... \right)$$

$$V_{OUT} = V_S \text{ for } V_+ > V_-$$

$$V_{OUT} = -V_S \text{ for } V_+ < V_-$$

$$V_{OUT} = V_{IN}$$

$$\text{slew rate} = \frac{\Delta V_{OUT}}{\Delta t}$$

$$\text{slew rate} = 2\pi f V_P$$

$$T = RC$$

$$V_C = V_0 e^{-\frac{t}{RC}}$$

$$V_C = V_0 \left(1 - e^{-\frac{t}{RC}} \right)$$

$$t = -RC \ln \left(1 - \frac{V_C}{V_0} \right)$$

$$t = -RC \ln \left(\frac{V_C}{V_0} \right)$$

$$f \approx \frac{1}{RC}$$

$$f = \frac{1}{T}$$

$$T = 1.1RC$$

$$t_H = 0.7 (R_1 + R_2) C$$

$$t_L = 0.7 R_2 C$$

$$f = \frac{1.44}{(R_1 + 2R_2) C}$$

$$\frac{T_{ON}}{T_{OFF}} = \frac{R_1 + R_2}{R_2}$$

$$V_r = \frac{I}{f_r C}$$

Candidate Name	Centre Number					Candidate Number				

AS ELECTRONICS

COMPONENT 1

Principles of Electronics

SAMPLE ASSESSMENT MATERIAL

2 hours 30 minutes

For Examiner's use only		
Question	**Maximum Mark**	**Mark Awarded**
1.	12	
2.	7	
3.	9	
4.	8	
5.	18	
6.	11	
7.	17	
8.	12	
9.	10	
10.	10	
11.	6	
Total	120	

ADDITIONAL MATERIALS

In addition to this examination paper,
you will require a calculator and a **Data Booklet**.

INSTRUCTIONS TO CANDIDATES

Use black ink or black ball-point pen.
Answer **all** questions.
Write your name, centre number and candidate number in the spaces at the top of this page.
Write your answers in the spaces provided in this booklet.

INFORMATION FOR CANDIDATES

The number of marks is given in brackets at the end of each question or part-question.
The assessment of the quality of extended response (QER) will take place in questions **7(a)** and **11**.

Answer **all** *questions.*

1. *(a)* Define capacitance. [1]

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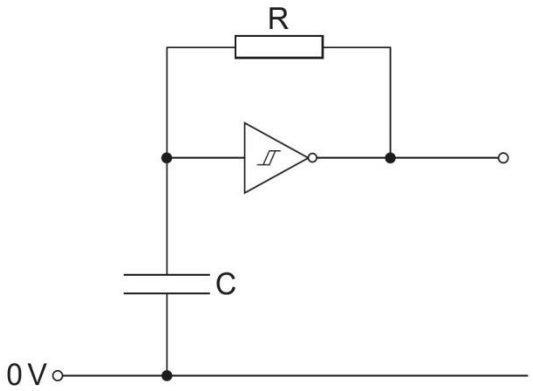
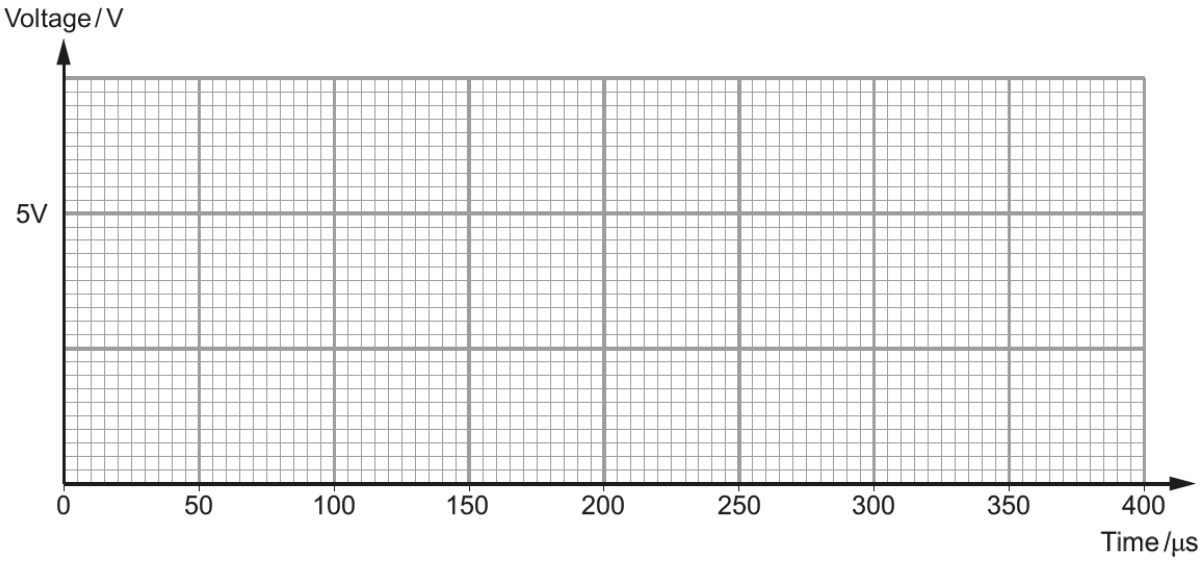
(b) The following diagram shows an astable sub-system based on a Schmitt inverter which is powered by a 5 V supply.



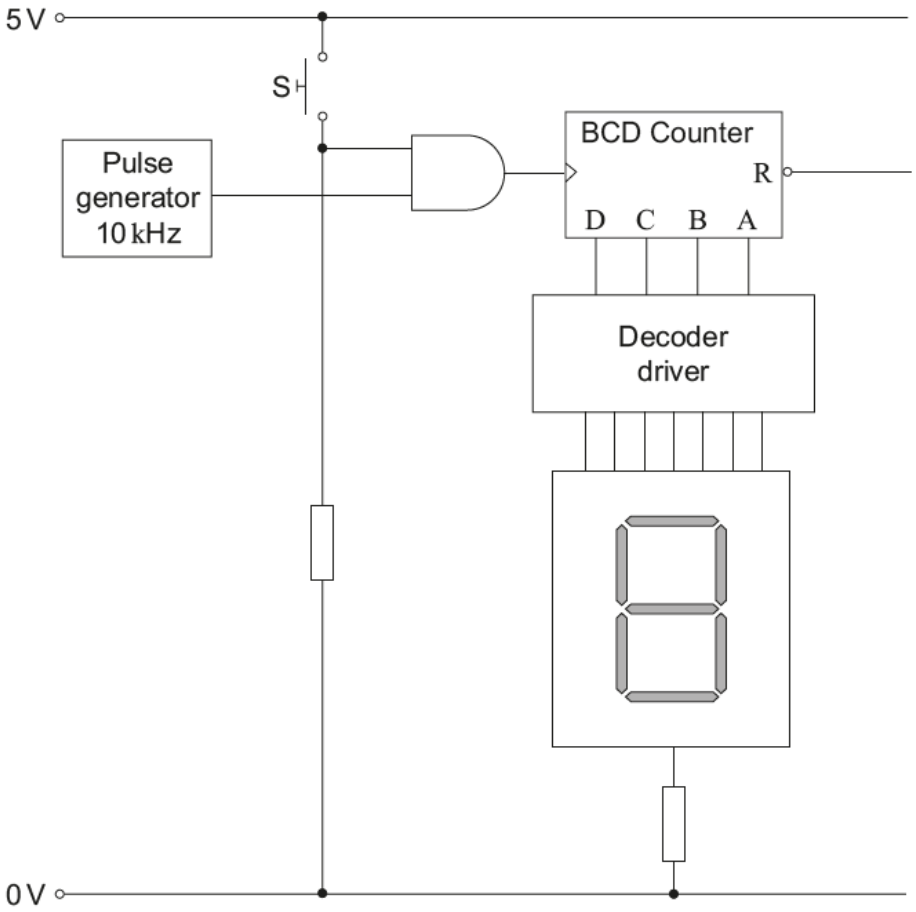
(i) Calculate the value for capacitor C to produce an output signal with a frequency of 10 kHz when R = 3.3 kΩ. [3]

capacitance = ... nF

(ii) Draw a graph on the grid belowto show two complete cycles of the astable waveform. [2]



The circuit diagram shows an incomplete simple random number generator that uses this astable.



(c) **Complete the circuit diagram** so that 5 is the largest number displayed. [3]

(d) Describe, in detail, what happens to the display when switch S is pressed for a few seconds and then released. [2]

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(e) State why a 1Hz astable is not suitable for this application. [1]

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2. A D-type flip-flop contains a number of logic gates. Each logic gate has a propagation delay. The clock input of the D-type goes through a transition gate that makes use of this propagation delay.

(a) State what is meant by a propagation delay and why a D-type flip-flop needs a transition gate on its clock input. [2]

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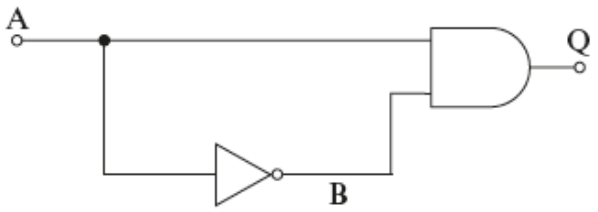
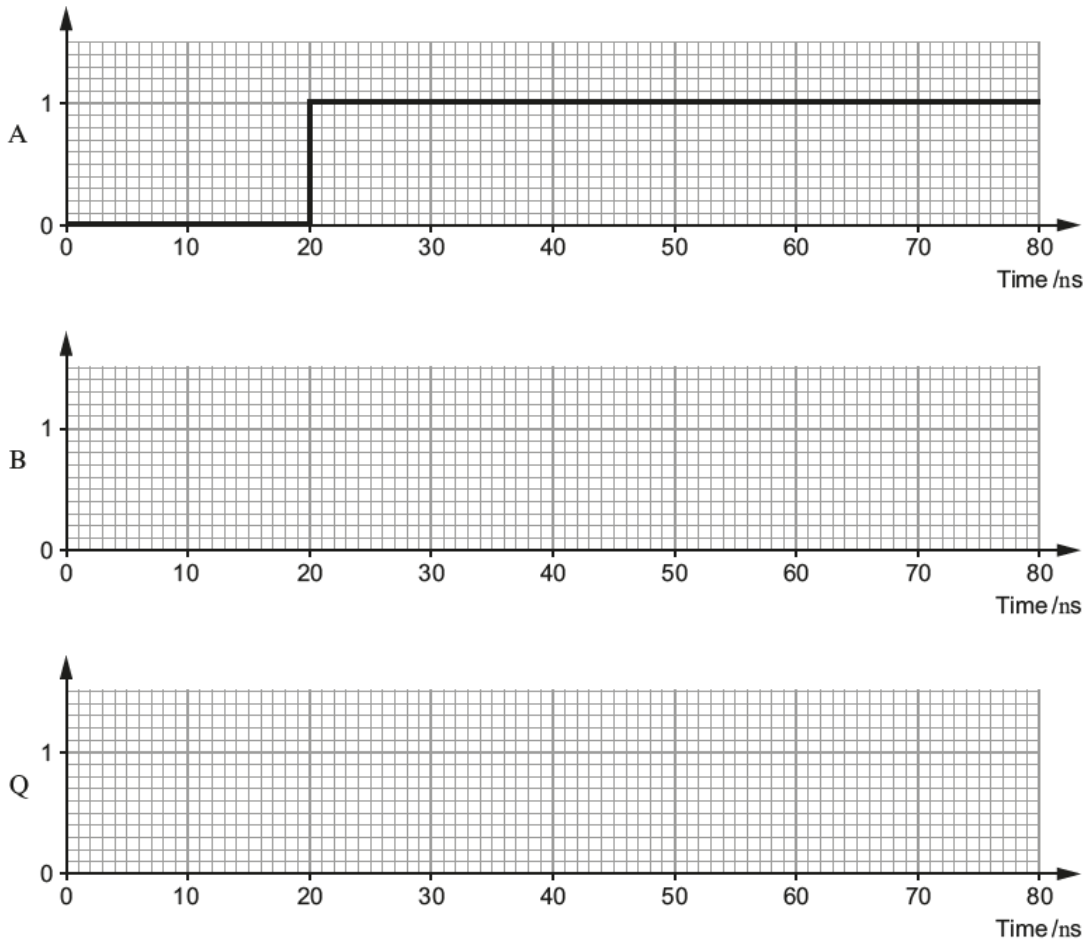
(b) A simple transition gate makes use of this propagation delay.
For each logic gate the propagation delay is 10 ns.



An input signal, shown on the timing diagram below is applied to input A.
Show on the diagram how the logic levels at **B** and **Q** change over the course of 80 ns. [3]



(c) Explain what changes to the signal at Q, if any, would occur if the logic gates in the above circuit were replaced by their NAND equivalents. [2]

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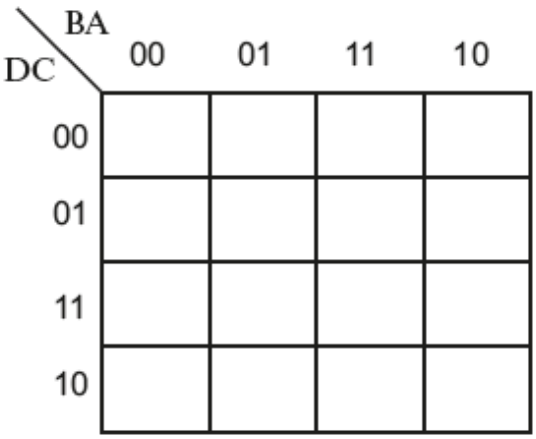
3. *(a)* Simplify the following expressions, showing appropriate working.

(i) $1 + B.\overline{A}$ = …….. [1]

(ii) $B.A + \overline{B}.A$ = …….. [1]

(b) Use a Karnaugh map to simplify the following expression as much as possible. [4]

$$\overline{D}.\overline{C}.\overline{B}.\overline{A} + D.C.A + \overline{D}.B.\overline{A} + \overline{D}.C.A$$



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(c) Apply DeMorgan's theorem to the following expression **and** simplify the result. [3]

$$Q = \overline{\overline{A}.B + \overline{B}}$$

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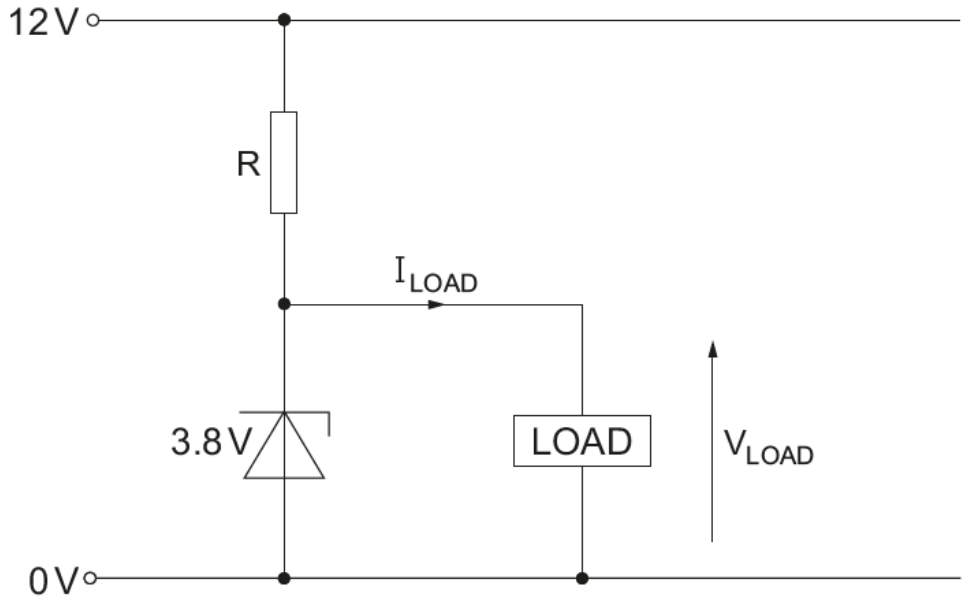
4. A simple 3.8 V regulated power supply is required for a portable electronic game to be used with a 12 V car battery.



The zener diode requires a **minimum** current of 10 mA to maintain the zener voltage.

(a) Calculate the ideal value for resistor R if the power supply is to supply load currents up to 350 mA and hence select the preferred value resistor that you would use from the E24 series. [4]

resistor R = ... Ω

(b) Calculate the power dissipated in the zener diode if the load is disconnected. [2]

power = ... W

(c) The output of the car battery varies and can reach 14.5 V.
When it is 14.5 V, describe what happens to the voltage across:

(i) resistor R [1]

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(ii) the load. [1]

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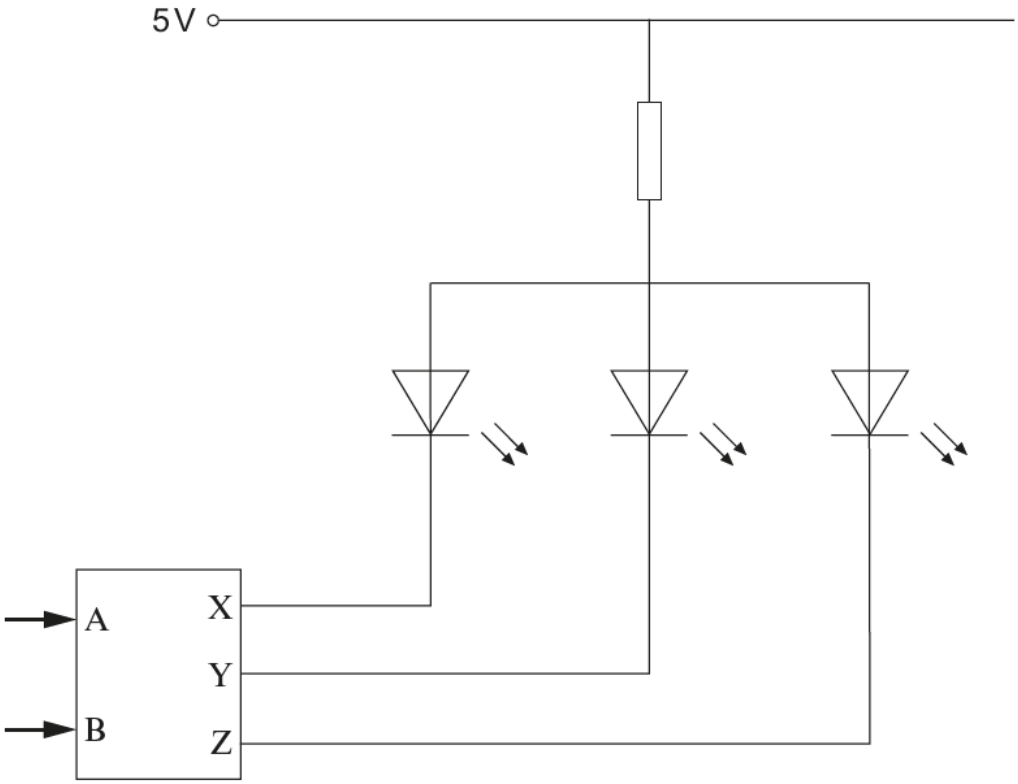
5. A student designs a system to convert a two-bit binary number into a bar chart by LED outputs coming on and staying on in succession.



The 3 LEDs are arranged in a row to form a bar the length of which indicates the size of the binary number.
An LED is lit when the corresponding output is at logic 0. The LED connected to X is the first in the bar.

(a) Complete the truth table to show how the outputs depend on the inputs. [3]

Input		Output		
B	A	X	Y	Z
0	0			
0	1			
1	0			
1	1	0	0	0

(b) Use the truth table to write down the Boolean expression for each of the outputs in terms of A and B. [3]

X = ……

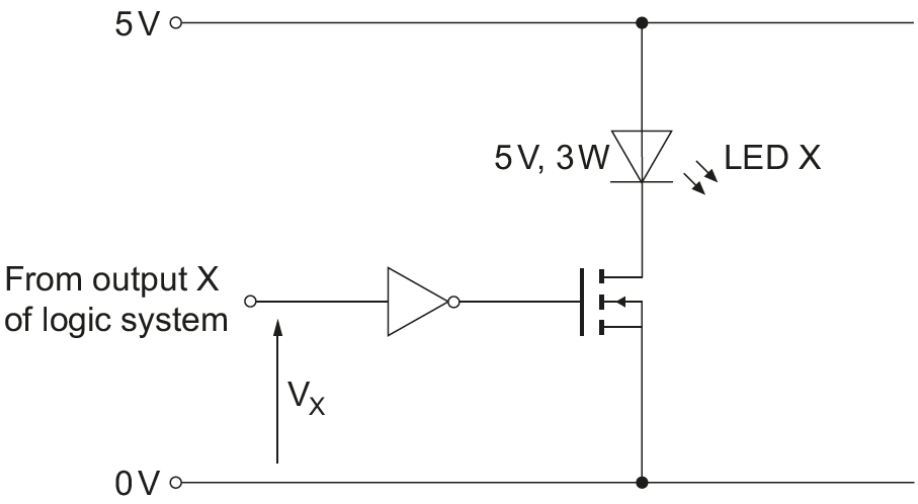
Y = ……

Z = ……..

(c) Draw a circuit diagram for the system using logic gates. [3]

(d) Redraw the system using NAND gates only. Credit will be given for using the minimum number of gates. [3]

(e) The student decides to make the display brighter by using high-power LEDs, each rated at 3 W. The modified output for LED X is shown below.



A MOSFET is used to interface the logic system to the high-power LED.

Calculate:

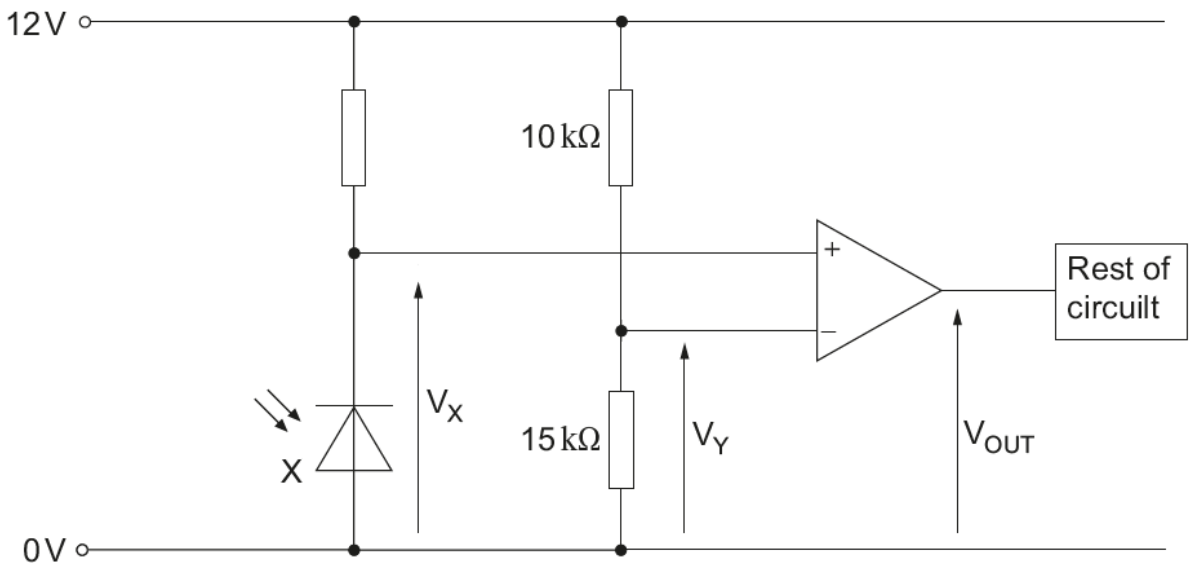
(i) the minimum value of g_m required to maintain this current when V_X is 5 V. [4]

g_m = ... S

(ii) the power dissipated in the MOSFET when the lamp is fully illuminated (r_{DSon} = 0.12 Ω). [2]

power = ... W

6. A factory engineer designs a control system to select and pack a set number of items from a conveyor belt. Each time an item passes a certain point a light beam is broken. The circuit diagram shows part of the sensing circuit.



(a) Describe what happens to the photodiode current as the light intensity changes. [1]

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(b) Calculate the voltage V_Y. [2]

Voltage V_Y = ... V

(c) With reference to V_X and V_Y explain why V_{OUT} changes when the light beam is broken. [4]

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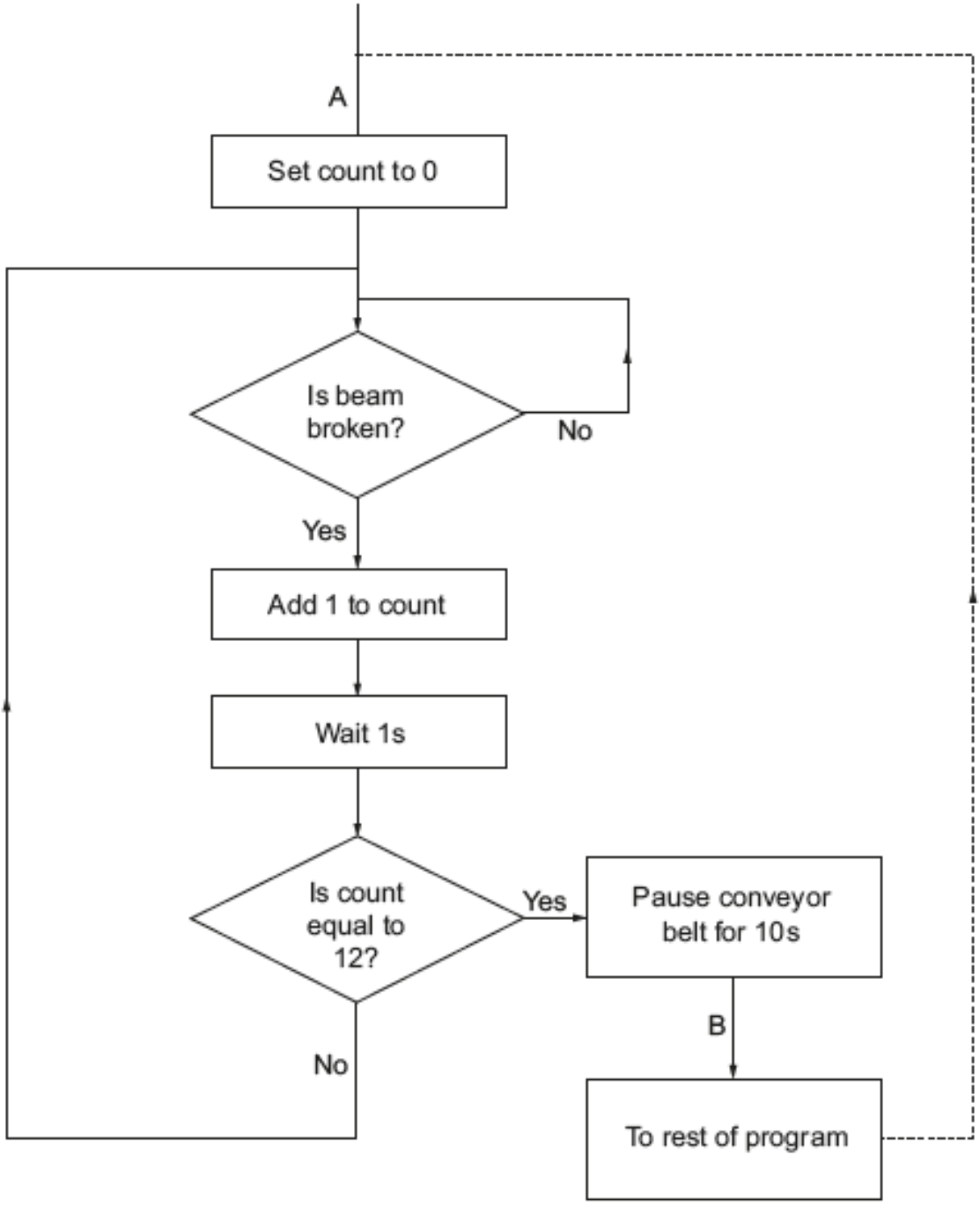
Here is part of the flowchart used to count the number of items passing through the light sensor.



(d) Explain what is happening between points A and B of the flow chart. [4]

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7. *(a)* Evaluate why feedback is used in voltage amplifiers built from op-amps used in audio amplifier systems. Give detail of how feedback is used in these systems. [6 QER]

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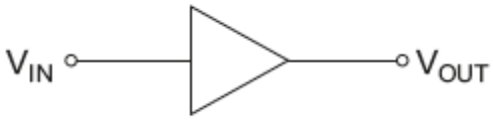
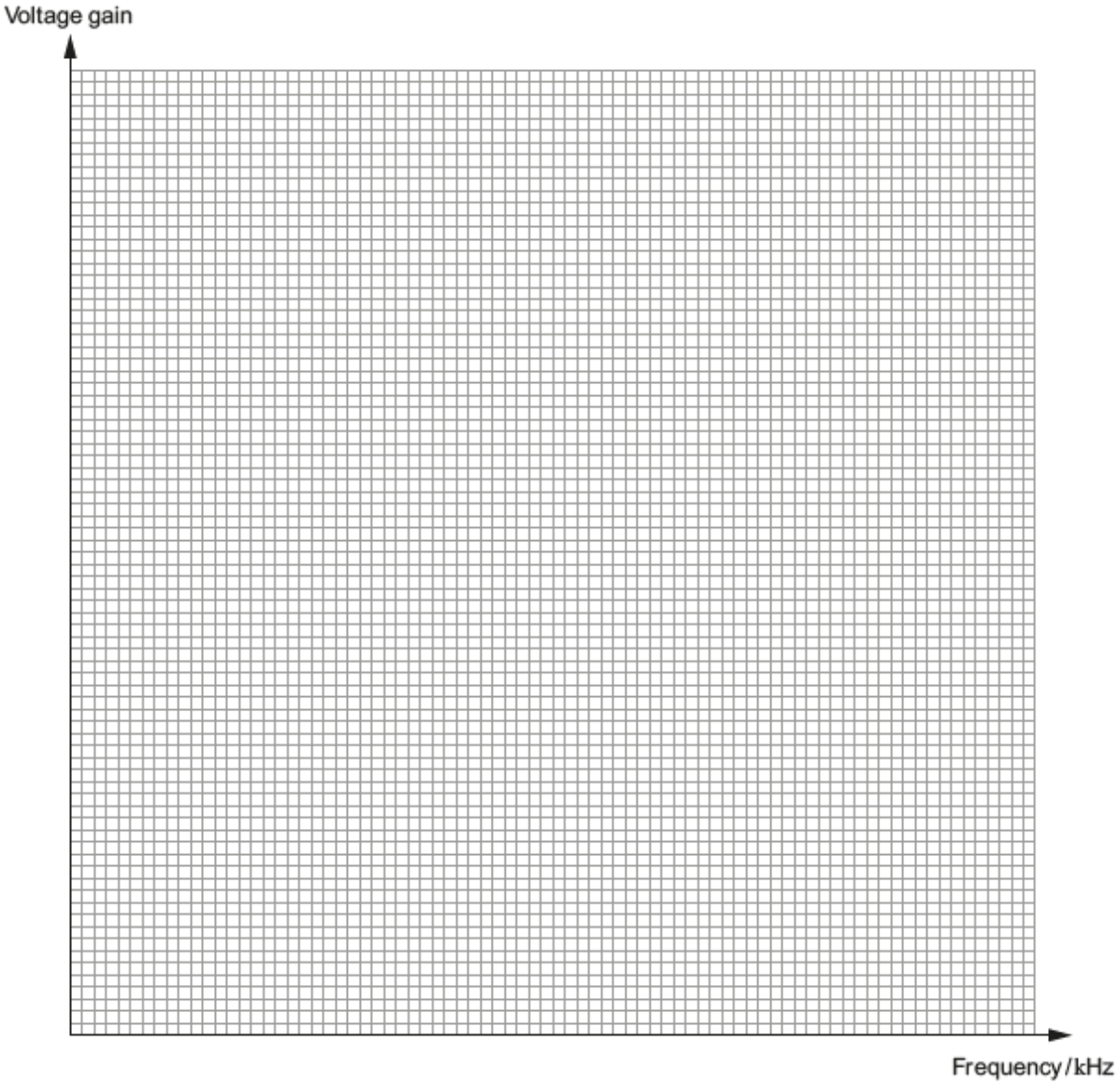
A student investigates the frequency response of a voltage amplifier based on an op-amp.



The following results were collected:

Frequency/kHz	**Voltage gain**
20	72.0
40	72.0
60	72.0
80	67.6
100	54.0
120	45.2
140	38.8
160	34.0

(b) Use the results to plot a graph of voltage gain against frequency. [3]



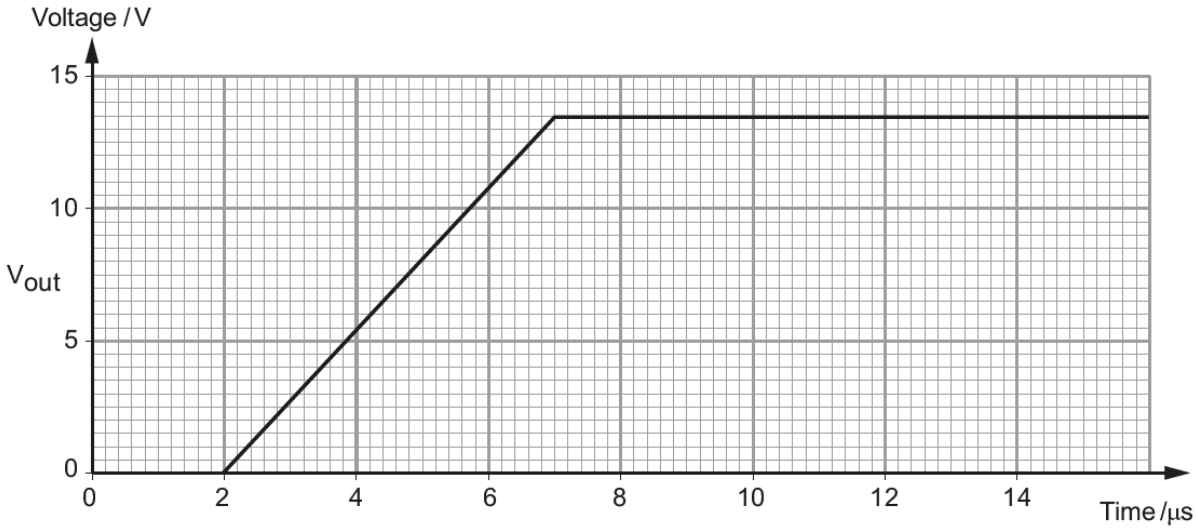
(c) Use the graph to estimate the bandwidth.
Show **on the graph** how you obtained your answer. [2]

Bandwidth = ... kHz

(d) Determine the gain-bandwidth product of the voltage amplifier. [2]

gain-bandwidth product = ... kHz

(e) The graph shows how the output voltage of the amplifier responds to a **large** step input voltage.



(i) Calculate the slew rate of this amplifier and give an appropriate unit. [2]

slew rate = ...

(ii) Describe with the aid of a sketch the effect of slew rate distortion on a sinusoidal waveform. [2]

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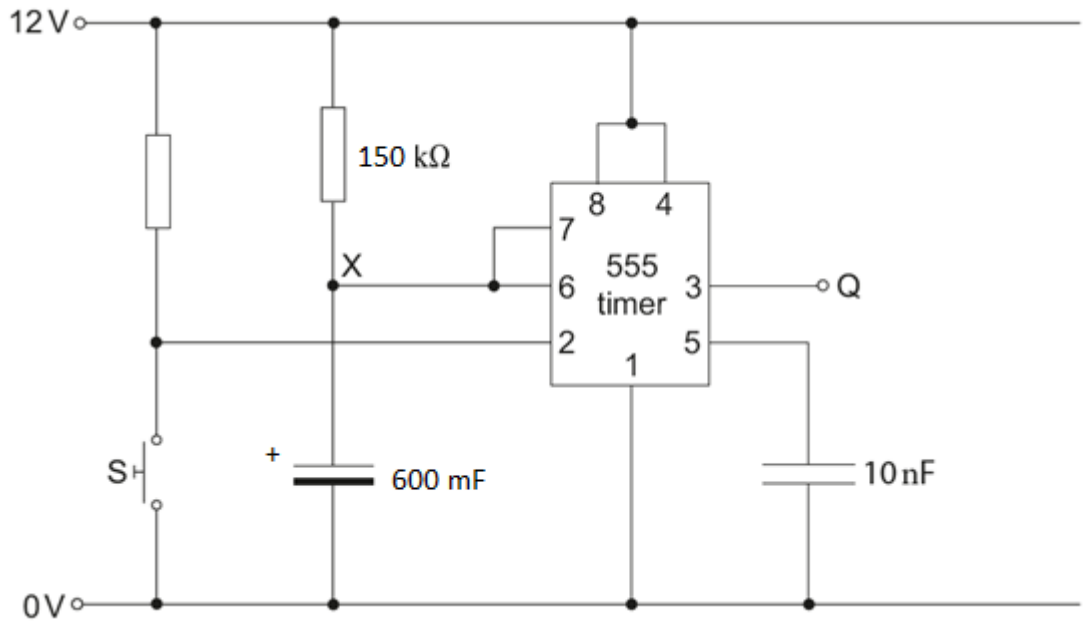
8. The diagram shows a monostable circuit based on a 555 timer.



Initially the timing capacitor is discharged. When S is momentarily pressed the timing capacitor begins to charge through the 200 kΩ resistor.

(a) Calculate:

(i) the time taken for the voltage at point X to reach 6 V; [3]

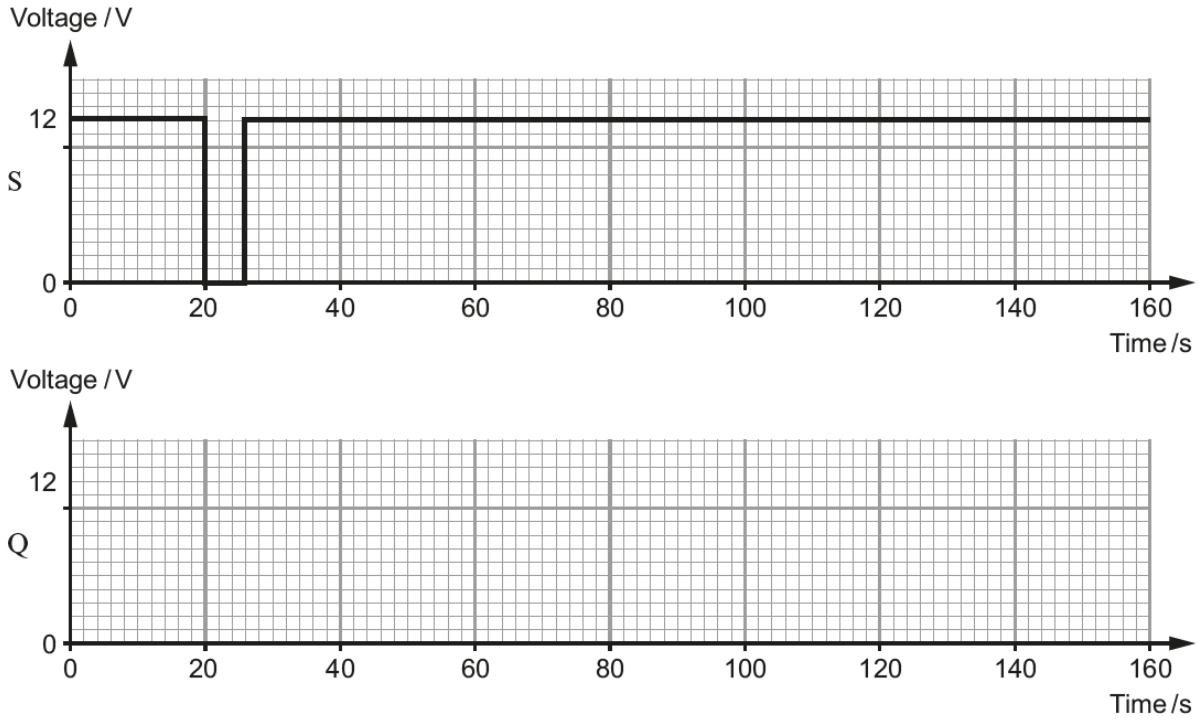
time = ... s

(ii) the voltage at point X after a time of 50 s. [3]

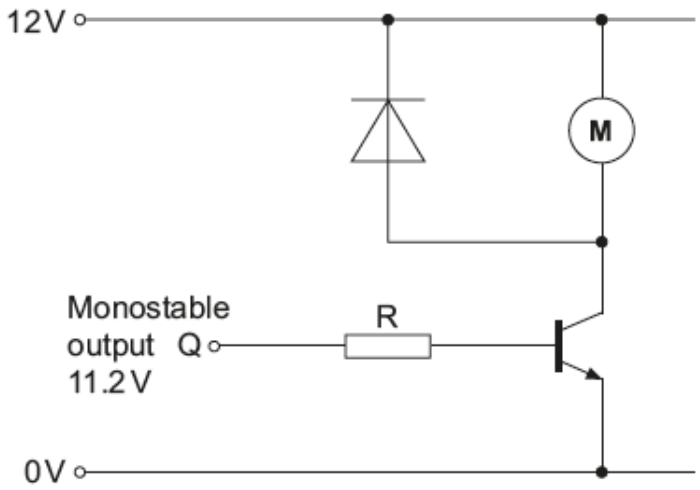
voltage = ... V

(b) The timing diagram shows the signal at pin 2 when switch S is momentarily pressed.

Complete the timing diagram for output Q. [2]



(c) The monostable is used to switch on a motor for a fixed period of time when switch S is momentarily pressed. A transistor switch is used to interface the monostable and the motor.



(i) State the purpose of the diode in this circuit. [1]

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The monostable output is 11.2 V and the current through the motor is 200 mA when the transistor is just saturated. The transistor has a current gain, h_{FE}, of 50.

(ii) Calculate the ideal value for resistor R. [3]

resistor R = ... Ω

9. *(a)* Design a circuit for a non-inverting voltage amplifier based on an op-amp with a voltage gain which is variable between 1 and 50.

The supply voltage is ± 18 V and the op-amp saturates at ± 17.5 V.

Draw the circuit diagram for the amplifier labelled with suitable component values. [5]

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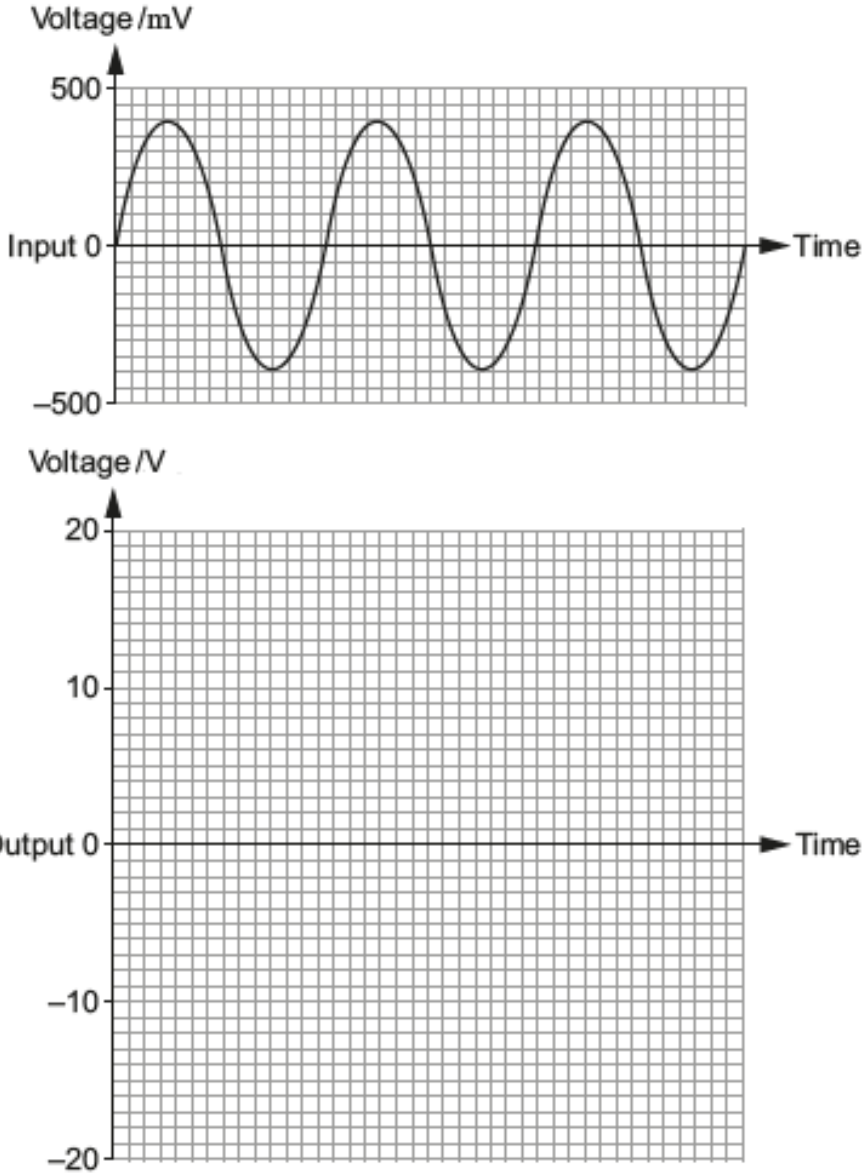
(b) (i) With the voltage gain set to 35 the following signal is applied to the amplifier input. Draw the output voltage on the axes provided. [2]



(ii) The input voltage remains unchanged.
Describe in detail what happens to the output as the gain is gradually increased to 50. [3]

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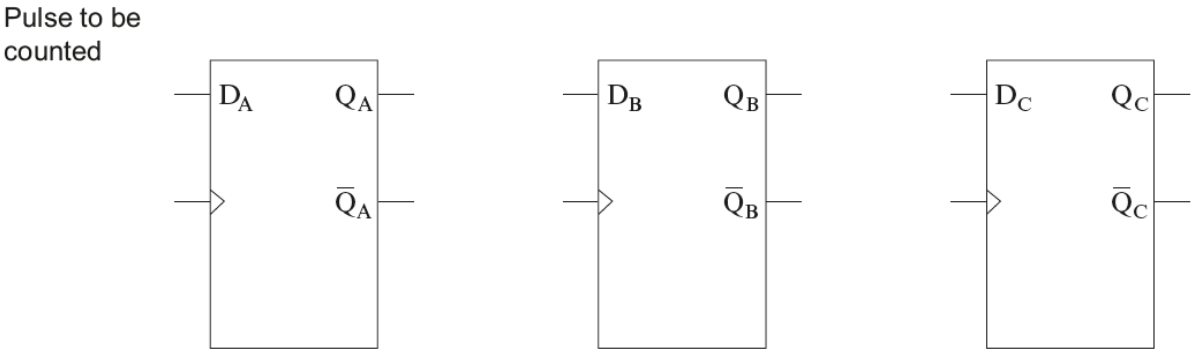
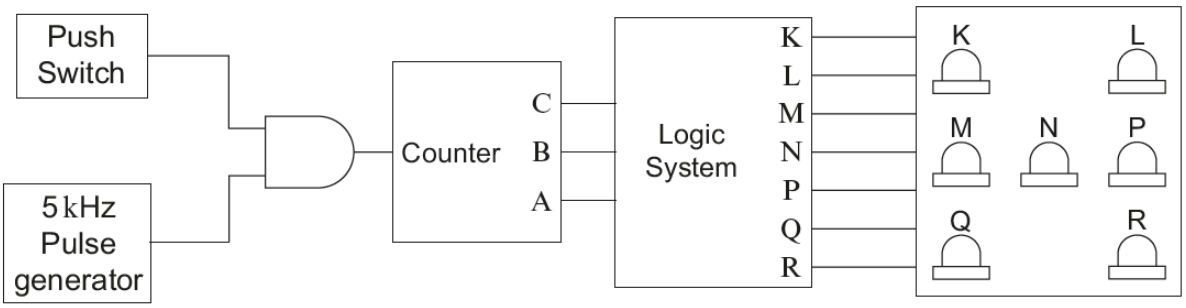
10. The diagram shows three D-type flip-flops which form part of a binary up-counter. Outputs A, B and C are used to indicate the binary output.
C is the most significant bit.

(*a*) Complete the diagram to make a 3-bit binary up-counter. Identify and label the outputs A, B and C. [3]



(b) The 3-bit counter is modified so that it resets on the sixth clock pulse and is used as part of the electronic dice game shown below.



An LED is on when the corresponding output is high.

When the push switch is pressed and held the LEDs flash in sequence.
When the switch is released the sequence stops with one to six LEDs on.

The truth table is used to show the sequence of outputs produced. Outputs K and R are the same and are shown in the table.
The remaining parts of the sequence are specified by the following Boolean expressions:

$$L = Q = C + B$$

$$M = P = C.\overline{B}.A$$

$$N = \overline{A}$$

(i) Complete the truth table to show the sequence of outputs produced. [3]

Clock pulse	C	B	A	K	L	M	N	P	Q	R
0	0	0	0	0						0
1	0	0	1	1						1
2	0	1	0	0						0
3	0	1	1	1						1
4	1	0	0	1						1
5	1	0	1	1						1
6	Counter resets here									

(ii) Write down the Boolean expression for output K. [1]

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(*c*) Output K of the logic system is at 5 V (logic 1) and illuminates the corresponding LED. Each LED operates with a forward voltage of 2.1 V and a current of 20 mA.

Draw a circuit diagram to show how the LED can be used to show the logic state of K and calculate the ideal value of the current limiting resistor. The LED should be on when K is sourcing a current. [3]

resistor R = ……..... Ω

11. Describe the procedure for determining the parameters of the Thevenin equivalent circuit for a power source by using standard test equipment. [6 QER]

END OF PAPER

AS ELECTRONICS

COMPONENT 1 – Principles of Electronics – SAMPLE PAPER

MARK SCHEME

GENERAL INSTRUCTIONS

Recording of marks

Examiners must mark in red ink.

One tick must equate to one mark (except for the extended response question).

Question totals should be written in the box at the end of the question.

Question totals should be entered onto the grid on the front cover and these should be added to give the script total for each candidate.

Marking rules

All work should be seen to have been marked.

Marking schemes will indicate when explicit working is deemed to be a necessary part of a correct answer.

Crossed out responses not replaced should be marked.

Credit will be given for correct and relevant alternative responses which are not recorded in the mark scheme.

Extended response question

A level of response mark scheme is used. Before applying the mark scheme please read through the whole answer from start to finish. Firstly, decide which level descriptor matches best with the candidate's response: remember that you should be considering the overall quality of the response. Then decide which mark to award within the level. Award the higher mark in the level if there is a good match with both the content statements and the communication statement.

Marking abbreviations

The following may be used in marking schemes or in the marking of scripts to indicate reasons for the marks awarded.

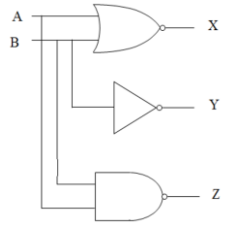
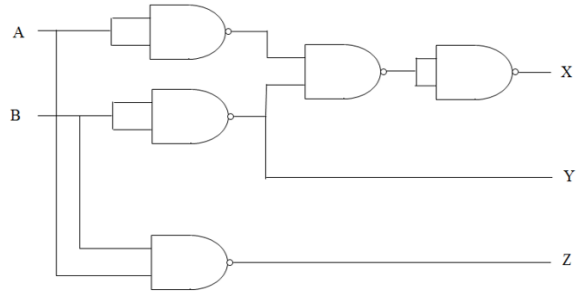
cao = correct answer only
ecf = error carried forward

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
1	*a*		$C=\frac{Q}{V}$	1			1	
	b	i	Values substituted into equation $f \approx \frac{1}{RC}$ (1) Correct algebra/manipulation $C=\frac{1}{Rf}=\frac{1}{(3.3\times10^{3}\times10\times10^{3})}$ (1) C = 3.03 x 10^{-8} = 30 [nF] (1)	1	1 1		3	3
		ii	2 complete cycles shown with equal mark-space ratio (1) Each complete cycle = 100 µs (1)	1	1		2	2
	c		B and C outputs chosen (1) NAND gate used (1) Output of logic gate to reset (1)	3			3	
	d		Whilst the switch is pressed the display cycles/ changes rapidly (1) When switch is released the display freezes/ stops changing/shows a single number (1) Don't accept reference to behaviour of counter	2			2	
	e		Too low a frequency **and** therefore you could see individual numbers/choose a number to stop at/not random		1		1	
			Question 1 total	**8**	**4**	**0**	**12**	**5**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
2	*a*		Propagation delay is the time taken for the output to respond to a change in input (1) A transition gate makes the D type edge-triggered (1)	2			2	
	b		B logic 1 at start (1) B changes from logic 1 to logic 0 from 30 ns to end (1) Q has [10 ns] pulse between 30 and 40 ns (1)		3		3	2
	c		The 10 ns pulse would shift along the time axis to between 40 and 50 ns (1) An extra 10 ns delay introduced because single AND gate is replaced by 2 NAND gates (1)		2		2	
			Question 2 total	**2**	**5**	**0**	**7**	**2**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
3	*a*	i	1	1			1	1
		ii	A	1			1	1
	b		All terms correctly mapped (1) Three groups correctly identified (**ecf** minimum no.) (1) Any correct term from groups identified (1) Simplest overall expression (**ecf**) (1) {$\overline{D}.\overline{B}.\overline{A} + C.A + \overline{D}.\overline{C}.\overline{A}$ or factorised version (**ecf**)}	1 1	1 1		4	4
	c		2 marks (one for each correct application of DeMorgan 1 mark simplification $\overline{\overline{(\overline{A}}.B.)}.B$ (1) $\overline{\overline{(\overline{A}}+\overline{B}).}B$ (1) $(A + \overline{B}).B$ $A.B$ (1)		3		3	3
			Question 3 total	**4**	**5**	**0**	**9**	**9**

Question			Marking details	Marks available				
				AO1	**AO2**	**AO3**	**Total**	**Maths**
4	*a*		12 – 3.8 = 8.2 V (1) 350 + 10 = 360 mA = 0.36 [A] (1) $R = \frac{V}{I} = \frac{8.2}{0.36}$ = 22.8 [Ω] (1) Preferred value 22 Ω. If the higher value 24 Ω were used the current would not reach 350 mA or converse argument (1)	1	1 1 1		4	1
	b		Substitution into equation P = VI = 3.8 x 360 (1) = 1368 [mW] accept 1.4 [W] (1)	1	1		2	2
	c	i	The voltage across the resistor increases / V_R = 14.5 – 3.8 = 10.6 V		1		1	
		ii	The output voltage remains constant / V_{LOAD} = 3.8 V		1		1	
			Question 4 total	**2**	**6**	**0**	**8**	**3**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
5	*a*		<table><tr><th colspan="3">Output</th></tr><tr><td>X</td><td>Y</td><td>Z</td></tr><tr><td>1</td><td>1</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table> 1 mark each column correct	3			3	
	b		$X = \overline{B}.\overline{A}$ $Y = \overline{B}$ 1 mark each correct expression $Z = \overline{B} + \overline{A}$ **ecf** from (a)		3		3	3
	c		 A and B connected to X via NOR gate (1) B connected to Y via NOT gate (1) A and B connected to Z via NAND gate (1) **ecf** from (a)	3			3	
	d		 NAND gate replacement of NOR correct (1) Remainder of circuit correct (but not minimised) (1) Minimum 5 gates used (1) **ecf** from (c)	1 1	1		3	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
	e	i	substitution into $P = IV = 3 = I \times 5$ (1) answer = 0.6 [A] (1) substitution into $I_D = g_M(V_{GS} - 3)$ = g_M= $\frac{0.6}{(5-3)}$ (1) g_m= 0.3 [s] (1)	1 1	1 1		4	4
		ii	selection and substitution $P = I^2R$ P = 0.6^2x 0.12 (1) P = 0.043 [W] accept (43 mW) (1)	1	1		2	2
			Question 5 total	**11**	**7**	**0**	**18**	**9**

Question			Marking details	Marks available				
				AO1	**AO2**	**AO3**	**Total**	**Maths**
6	*a*		As the light intensity increases the photocurrent increases Or converse argument	1			1	
	b		Substitution $V_{OUT} = \frac{R_2}{R_1 + R_2} V_{IN} = \frac{15}{(10+15)} \times 12$ (1) Correct answer 7.2 V (1)	1	1		2	2
	c		In bright light $V_Y > V_X$ (1) therefore $V_{OUT} \approx 0$ V (1) As light intensity decreases V_X increases until it exceeds V_Y (7.2 V) (1) therefore $V_{OUT} \approx 12$ V (1)		4		4	
	d		Explanation identifies main functions of the flowchart. • Flowchart checks to see if light beam is broken (1) • Light beam broken 12 times before conveyor belt is paused for 10 seconds – counter and decisions used forming a loop. Counter set to zero at start of program (from point A).(1) • 1 second delay between each count - each time an item breaks the beam 1 is added to count and there is a 1 s delay (1) • After conveyor belt is paused for 10 seconds the flowchart returns to the rest of the program (1)	4			4	
			Question 6 total	**6**	**5**	**0**	**11**	**2**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
7	*a*		**Indicative Content:** **A01 allocation -** Voltage amplifiers built from op-amps use negative, resistive feedback. **A03 allocation -** Without negative feedback the output of the amplifier would be driven into saturation by very small changes in the input voltage. Negative feedback is achieved by connecting a resistor between the output and the inverting input. The effect of negative feedback is to increase the stability of the amplifier by reducing the gain (from the very high open-loop value) and this in turn increases the bandwidth. The greater the value of the resistor in the feedback loop (relative to the input resistor) the higher the gain and the lower the bandwidth. Choosing the resistor values allows the user to achieve a specific voltage gain using standard formulae. **5-6 marks** Clearly states that voltage amplifiers use negative feedback and/or uses diagrams to show how negative feedback is achieved. Explains that choosing resistor values allows the user to achieve a specific gain using standard formulae. The greater the value of resistor in the feedback loop relative to the input resistor the higher the gain and the higher the gain the lower the bandwidth. *There is a sustained line of reasoning which is coherent, substantiated and logically structured. The information included in the response is relevant to the argument.* **3-4 marks** States or implies voltage amplifiers use negative feedback and/or uses diagrams to show how negative feedback is achieved. Some reference made to how resistance values effect voltage gain. Some reference to bandwidth. *There is a line of reasoning which is partially coherent, supported by some evidence and with some structure. Mainly relevant information is included in the response but there may be some minor errors or the inclusion of some information not relevant to the argument.*	1		5	6	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
			1-2 marks States or implies voltage amplifiers use negative feedback and/or uses diagrams to show how negative feedback is achieved. Some link made between resistance values and voltage gain or some reference to bandwidth. *There is a basic line of reasoning which is not coherent, supported by limited evidence and with very little structure. There may be significant errors or the inclusion of information not relevant to the argument.* **0 marks** *No attempt made or no response worthy of credit.*					
	b		Appropriate scales, no multiples of 3 (1) All points correctly plotted ± ½ small square division (1) Correct line plotted no tolerance (1)		3		3	3
	c		Line across at $\frac{72}{\sqrt{2}} = 51$ and down to frequency axis (1) 108 ± 2 [kHz] (1)		2		2	2
	d		72x108 correct substitution (1) = 7 776 [kHz] accept 7.8 MHz (range 7920 to 7632) **ecf** (1)	1	1		2	2
	e	i	$\text{slew rate} = \frac{\Delta V_{OUT}}{\Delta t} = \frac{13.5}{5}$ correct substitution (1) $2.7 V\mu s^{-1}$ **appropriate unit with numerical answer** (1) accept $2.7\ MVs^{-1}$	1	1		2	2
		ii	[At low frequencies the sine wave is unaltered for both small and large amplitude signals] For large signals, as the frequency increases the sine wave becomes a triangular wave (1) then ***either*** The amplitude of the triangular wave decreases further as the frequency increases / the amplitude is further increased / The gradient of the triangular wave equals the slew-rate (1)			2	2	
			Question 7 total	**3**	**7**	**7**	**17**	**9**

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
8	*a*	i	RC =150 × 10^3 × 600 × 10^{-6} = 90 s (1) Substitution: $t = -RC\ln\left(1-\frac{V_C}{V_0}\right)$ = $T_{1/2}$= 90 x ln2 (1) = 62.4 [s] (1)	 1	1 1		 3	 3
		ii	Selection of correct formula to use (1) correct substitution $V_X = 12(1-e^{-(50/90)})$ (1) = 5.1 [V] (1) **ecf** on time constant	1 1	 1		 3	 2
	b		Monostable pulse starting at falling edge of S (1) Correct duration i.e. $T = 1.1RC$ = 1.1 × 90 = 99 s (1)		 2		 2	 1
	c	i	To prevent negative voltage spikes/to prevent back e.m.f's damaging the transistor/ to clamp the collector to 0.7 V of supply	1			1	
		ii	$I_C = h_{FE} I_B$ $I_B = \frac{200}{50}$ = 4 mA (1) V_R = 11.2 – 0.7 = 10.5 V (1) $R = \frac{V}{I} = \frac{10.5}{4\times10^{-3}}$ = 2 625 [Ω] accept 2.6 kΩ (1)	 1	1 1		 3	 2
			Question 8 total	**5**	**7**	**0**	**12**	**8**

Question			Marking details	Marks available				
				AO1	**AO2**	**AO3**	**Total**	**Maths**
9	*a*		V_{IN} connected directly to the non-inverting input (1) Inverting input connected to 0 V (1) **Variable** resistor connected between inverting input and output (1) Resistances in the ratio 49 :1 with R_F correctly identified (1) Both resistances ≥ 1 kΩ (1)		1 1	1 1 1	5	1
	b	i	Output sine wave with same phase and frequency as input (1) Peak correct with labelled axis i.e. 14 V (1) (allow peak labelled directly as 14 V)	2			2	2
		ii	Sine wave increase in amplitude at start (1) Frequency and phase remain unchanged (1) When output reaches 17.5 V the top of the wave is clipped (1)	3			3	
			Question 9 total	**5**	**2**	**3**	**10**	**3**

<table>
<tr><th colspan="3" rowspan="2">Question</th><th rowspan="2">Marking details</th><th colspan="4">Marks available</th><th></th></tr>
<tr><th>AO1</th><th>AO2</th><th>AO3</th><th>Total</th><th>Maths</th></tr>
<tr><td>10</td><td>a</td><td></td><td>Each $\overline{Q}$ connected to its corresponding D input x 3 (1)
Each Q connected to its corresponding labelled output terminal x 3 (1)
All clock connections correct (1)</td><td>3</td><td></td><td></td><td>3</td><td></td></tr>
<tr><td></td><td>b</td><td>i</td><td>
<table>
<tr><th>K</th><th>L</th><th>M</th><th>N</th><th>P</th><th>Q</th><th>R</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
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<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Column L and Q correct (1)
Column M and P correct (1)
Column N correct (1)</td><td></td><td>3</td><td></td><td>3</td><td>3</td></tr>
<tr><td></td><td></td><td>ii</td><td>C + A</td><td>1</td><td></td><td></td><td>1</td><td>1</td></tr>
<tr><td></td><td>c</td><td></td><td>LED and series resistor connected between K input and O V (Correct symbols and LED orientation needed) (1)
V + 5 – 2.1 = 2.9 V (1)
$R = \frac{V}{I} = \frac{2.9}{0.02}$ = 145 Ω accept 0.145 kΩ (1)</td><td>1</td><td>1
1</td><td></td><td>3</td><td>1</td></tr>
<tr><td></td><td></td><td></td><td>Question 10 total</td><td>5</td><td>5</td><td>0</td><td>10</td><td>5</td></tr>
</table>

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
11			**Indicative Content:** **AO1 allocation -** Thevenin's theorem allows more complex power sources to be replaced by a single pair of supply rails and a resistor. This is called the equivalent circuit. **AO3 allocation -** The voltage across the power rails V_{OC} is found experimentally by connecting a voltmeter between the positive terminal and 0 V and noting the reading. The value of the resistor, R_{EQ} is determined using the short-circuit current. This is found by connecting an ammeter between the positive terminal and 0 V and noting the reading [high current range meter needed]. R_{EQ} is calculated by dividing the open-circuit voltage by the short-circuit current. The equivalent circuit is drawn using the open-circuit voltage V_{OC} as the supply voltage and the resistor R_{EQ} in series with this voltage terminal and the output. **5-6 marks** Describes and/or draws the equivalent circuit as two supply rails and a resistor. A description uses correct terminology for V_{OC} and I_{SC} to describe how to measure these using a voltmeter and ammeter. Detailed description shows the formula used to calculate R_{EQ} and that V_{OC} is the supply voltage for the equivalent circuit. *There is a sustained line of reasoning which is coherent, substantiated and logically structured. The information included in the response is relevant to the argument.*	1		5	5	

Question			Marking details	Marks available				
				AO1	AO2	AO3	Total	Maths
			3-4 marks Partially correct method (in a description and/or diagram) of obtaining V_{OC} and I_{SC} given but lack of detail and/or terminology missing. Some attempt to calculate a resistance but no clear idea of what this resistor represents in the equivalent circuit or that V_{OC} is the supply voltage. *There is a line of reasoning which is partially coherent, supported by some evidence and with some structure. Mainly relevant information is included in the response but there may be some minor errors or the inclusion of some information not relevant to the argument.* **1-2 marks** Some attempt (in a description and/or diagram) at measuring either the voltage or current but no method present. No real understanding of how to use the results or incorrect use of resistance formula. Unable to explain the equivalent circuit. *There is a basic line of reasoning which is not coherent, supported by limited evidence and with very little structure. There may be significant errors or the inclusion of information not relevant to the argument.* **0 marks** *No attempt made or no response worthy of credit.*					
			Question 11 total	**1**	**0**	**5**	**6**	**0**
			TOTAL	**52**	**53**	**15**	**120**	**55**