GCE A LEVEL EXAMINERS' REPORTS

ELECTRONICS
A LEVEL

SUMMER 2023

Introduction

Our Principal Examiners' reports offer valuable feedback on the recent assessment series. They are written by our Principal Examiners and Principal Moderators after the completion of marking and moderation, and detail how candidates have performed.

This report offers an overall summary of candidates' performance, including the assessment objectives/skills/topics/themes being tested, and highlights the characteristics of successful performance and where performance could be improved. It goes on to look in detail at each question/section of each component, pinpointing aspects that proved challenging to some candidates and suggesting some reasons as to why that might be.[i]

The information found in this report can provide invaluable insight for practitioners to support their teaching and learning activity. We would also encourage practitioners to share this document – in its entirety or in part – with their learners to help with exam preparation, to understand how to avoid pitfalls and to add to their revision toolbox.

Further support

Document	Description	Link
Professional Learning / CPD	Eduqas offers an extensive annual programme of online and face-to-face Professional Learning events. Access interactive feedback, review example candidate responses, gain practical ideas for the classroom and put questions to our dedicated team by registering for one of our events here.	https://www.eduqas.co.uk/home/professional-learning/
Past papers	Access the bank of past papers for this qualification, including the most recent assessments. Please note that we do not make past papers available on the public website until 6 months after the examination.	www.wjecservices.co.uk or on the Eduqas subject page
Grade boundary information	Grade boundaries are the minimum number of marks needed to achieve each grade. For unitised specifications grade boundaries are expressed on a Uniform Mark Scale (UMS). UMS grade boundaries remain the same every year as the range of UMS mark percentages allocated to a particular grade does not change. UMS grade boundaries are published at overall subject and unit level. For linear specifications, a single grade is awarded for the overall subject, rather than for each component that contributes towards the overall grade. Grade boundaries are published on results day.	For unitised specifications click here: Results and Grade Boundaries (eduqas.co.uk)

Exam Results Analysis	WJEC Eduqas provides information to examination centres via the WJEC secure website. This is restricted to centre staff only. Access is granted to centre staff by the Examinations Officer at the centre.	www.wjecservices.co.uk
Classroom Resources	Access our extensive range of FREE classroom resources, including blended learning materials, exam walk-throughs and knowledge organisers to support teaching and learning.	https://resources.eduqas.co.uk/
Bank of Professional Learning materials	Access our bank of Professional Learning materials from previous events from our secure website and additional pre-recorded materials available in the public domain.	www.wjecservices.co.uk or on the Eduqas subject page.
Become an examiner with Eduqas.	We are always looking to recruit new examiners or moderators. These opportunities can provide you with invaluable insight into the assessment process, enhance your skill set, increase your understanding of your subject and inform your teaching.	Exam Marking jobs | Examiner & Moderator Vacancies From Eduqas

Subject Officer's Executive Summary

The component 1 and component 2 examination papers overall performance was in line with previous years, with similar levels of difficulty. The standard deviation of marks for all three components was very similar to the 2019 series.

The NEA reports were again presented to a high standard by most candidates with many complex systems being realised.

Areas for improvement	Classroom resources	Brief description of resource
Manipulation of equations including multipliers	Electronics eBook resources	Chapters cover the content of the specification with worked examples, exercises and practical investigations for each topic.
Familiarity with sub-systems covered in the specification and their applications.	Electronics eBook resources Knowledge organisers	Component 1, Chapter 1 covers recognition and design of systems from sub-system blocks with worked examples, exercises and practical investigations for each topic. A good revision starting point.
Quality of response (QER) question approach.	Electronics eBook resources Past papers and mark schemes	Chapters cover the content of the specification with worked examples, exercises and practical investigations for each topic. Past papers and mark schemes contain many examples of QER questions and model answers.
NEA – The specification should give details of the individually chosen problem which is drawn from the analysis of research into the problem.	Electronics as specification 2019 and 2020 CPD material	Overview of the NEA and marking criteria. 2019 and 2020 CPD material on the secure website contains commentary from previous series and examples of work.
NEA – Circuit diagrams and circuit simulations of sub-systems are only valid if real components such as LM741 or BC548 are chosen rather than the generic IC1 and Q1.	2019 and 2020 CPD material	2019 and 2020 CPD material on the secure website contains commentary from previous series and examples of work.

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COMPONENT 1: PRINCIPLES OF ELECTRONICS

Overview of the Component

This component contained a broad coverage of content from the core and across all topics of component 1 with some synoptic elements in questions 4, 7 and 11. Questions contained a balance of recall, application of knowledge and design and evaluation.

Some candidates were able to produce excellent responses across all topics and types of questions. Other candidates were stronger in some topics than others, this was particularly the case with combinational logic questions having stronger responses. It was evident that questions requiring recall demonstrated that some candidates were better prepared for some topics than others. The questions that required application of knowledge demonstrated that whilst many candidates demonstrated some level of skill in this, some found it more difficult to apply their knowledge to an unfamiliar application of a system. In questions where a mathematical response required the manipulation of a formula there was a range in quality of responses with some accurate and excellently laid out, and others where candidates were unable to carry out the necessary manipulation. Written explanations again displayed a range of quality in responses from clear and well-structured to minimal and poorly structured.

The paper was of a similar standard to previous years with a slightly higher mean mark than in 2019 and 2022.

Comments on individual questions/sections

Q.1 Generally well answered, although some were confused by the logic gate sinking the LEDs current. (Facility factor 0.82)

Q.2 This questioned many aspects of combinational logic and candidates were generally very successful in providing clear written and well-drawn responses. Where there were minor errors a minimum of marks was lost with error carried forward being applied. (Facility factor 0.83)

Q.3 This question dealt with the application of standard circuit analysis calculations and most candidates demonstrated that they were able to apply these. However the introduction of a diode confused many candidates, thus reducing their success in applying their knowledge. This was particularly true of parts (a)(ii) and (iii). (Facility factor 0.41)

Q.4 Part (a) proved to be an excellent discriminator and there was a whole range of marks from 0 to 6. Many candidates were able to interpret the circuit accurately although the use of a D-type as a frequency divider was missed by some. Part (b) focussed on the application of a multiplexer in a communications system. Many candidates gave a good explanation in part (ii) however many others struggled with written explanations.

Q.5 No specific areas to highlight.

Q.6 This question was accessible to the majority of candidates. However, whilst there were some excellent answers the rearrangement of the formula required in 6 (c) was challenging for some candidates.

Q.7 The application of the Thevenin circuit once derived in 7 (a)(ii) was another part where many candidates were unable to apply the relevant mathematical solution.

Q.8 Only 96.8% of candidates attempted this question, the lowest in this paper. However the facility factor, 0.69, indicates that those that did performed well.

Q.9 Many candidates were unable to draw correct diagrams in parts (a)(i) and (b)(i). In part (c) there were a significant number of candidates who missed the word “different” in the stem and therefore applied values from part (b) in their calculations. Many candidates were able to identify the correct equation but were unable to identify the correct values for the quantities in these equations.
(Facility factor 0.41)

Q.10 This question included the QER response. As in other parts of the paper there were some excellent responses very worthy of the full 6 marks. However, many candidates produce low quality answers, and further practice of these is clearly needed. The best responses were written in a logical and structured manner based on a clear plan whereas other responses were a collection of knowledge put down in a manner that lacked structure and clarity.

Q.11 No specific areas to highlight.

Q.12 No specific areas to highlight.

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COMPONENT 2: APPLICATION OF ELECTRONICS

Overview of the Component

The demands of the paper and the general performance of candidates were very much in line with those of previous years. This component contained broad coverage of content from the core and across all topics of component 2 with some synoptic elements. Questions contained a balance of recall, application of knowledge and design and evaluation.

Mathematical questions produced better results than those requiring explanation or description. Still a number of candidates tried to draw accurate circuit diagrams and graphs 'freehand', though the use of pencils was more widespread than in some years.

Comments on individual questions/sections

Q.1 The calculations were well-answered, though some quoted the mark/space ratio as 1:2. The outputs P, X, Y and Z were usually correct, but few took any notice of the reset circuit.

Q.2 Part (a) was usually answered correctly (though not always with the help of a ruler) the common mistake was to ignore the effect of the 'Set' input. Part (b)(ii) most candidates identified the main sequence in, but some missed the unused states resulting in a loss of marks in part (iii). Answers to part (iv) often lacked clarity and rarely mentioned the significance of 'power-up'.

Q.3 Generally answered very well, although some confusion between the register PORTA and TRISA was seen. Quite a few thought that the bits in the registers were numbered '1' to '8' rather than '0' to '7'.

Q.4 Many good answers were seen to part (a), however some had four diodes but not connected in a bridge, incorrect orientation of diodes, incorrect output connections to the capacitor. Many candidates in part (b) failed to specify whether 'regulated output' referred to voltage or current.

Q.5 In this QER question, some candidates produced well planned and cogent analysis of the system, with valid comments on its suitability to meet the specification. However, some failed to see the error in the monostable circuit.

Q.6 In part (a) and (b)(i) some candidates used the wrong formulae or failed to show correct use of the multipliers involved. Many candidates failed to design a divide by four circuit with many using three or four D-type flip-flops in their answer, or ignored the Q bar to D connections, or used a common clock connection.

Q.7 Generally well-answered apart from the graph, with some choosing the wrong characteristic for the bass-cut filter and many ignored the 450 roll-off.

Q.8 Part (b) showed many good answers that mentioned Nyquist's theorem, though a few worked the calculation in the wrong direction and derived the answer of 20kHz. Part (c) was generally well answered with better responses that mentioned removing the noise added during transmission down the comms. link. Part (c)(ii) answer required a reference to quantisation noise.

Q.9 Generally well answered although there were many vague answers that revealed common misunderstandings of optical fibres. The circuit design in part (c) was not well answered, many forgot the switch unit, or the common clock connections.

Q.10 Part (a) was generally well answered, although in part (iv) most recognised that pressing switch S2 created reverse bias but were unable to describe how this happened. In part (b)(i) only a few candidates were able to complete the circuit diagram correctly, but the remainder of the question was generally very well-answered.

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COMPONENT 3: SYSTEM DESIGN AND REALISATION TASKS – NEA

Overview of the component

This component required each learner to complete two tasks independently. The tasks built on the concepts studied throughout the course and the requirement to relate practical circuit design and realisation to knowledge and understanding gained from the study of components 1 and 2.

Task 1 (20 marks) – involved the development of a microcontroller system programmed through assembler language.

Task 2 (50 marks) – was a substantial system development including analogue and digital sub-systems in an integrated design.

Each task enabled candidates to carry out a design and realisation task based on an individually identified problem, context or opportunity.

Centres are to be congratulated for their effort in presenting candidates' work for moderation, including the online recording of centre marks. Candidates in the majority of centres provided excellent photographic evidence.

Tasks
Comments on tasks/questions relating to candidate performance/meeting assessment criteria

Candidates should focus on a problem to analyse to enable them to write a design specification based on a specific identified problem.

Many candidates struggled to provide meaningful parameters and simply quoted power supply values, current consumption and cost without any justification. A full specification should include measurable parameters and numerical data justified by analysis of relevant research of the problem.

An increasing number of candidates had ideal components rather than real in their circuit diagrams. Real components model real circuit behaviour and are required to provide an accurate high quality and fully labelled circuit diagram.

A common weakness in both tasks was in the Evaluation section. To gain the full range of marks for the evaluation candidates must make valid, critical and objective evaluation of the performance of the complete system. The evaluation should compare the system with the design specification. A poor evaluation was often the consequence of having few realistic measurable parameters in the specification which then resulted in some simplistic evaluations.

Suggestions for improvement must be relevant and should state why incorporating such an improvement would be beneficial rather than simply mentioning better coding or better light sensors.

Task 1
For the microcontroller task at A level, candidates are required to program the microcontroller using assembly language, other programming languages are not acceptable.

It was pleasing to see that this year no centres allowed candidates to produce hybrid programs that included both assembler and Basic commands (be aware: this is possible within PICAXE).

A number of centres submitted microcontroller projects containing light sequences which resulted in all candidates within the centre producing very similar programs. As the tasks are from individual problems identified by the candidates, it would be expected that specification parameters would usually be different, and programs would have variations in structure and commands used.

Credit cannot be awarded for commands used to configure the ports. However, credit can be given should these same commands be used by the candidate in their main program and any sub-routine they write.

A few centres were not using the 'Assembly Language Template' provided on our website. It is important that centres use this template. All standard sub-routines are listed in it and any sub-routines called and equate statements used should be included in the task 1 template. It is important that candidates realise that these sub-routines and equate statements actually exist.

Task 2
A project should consist of sub-systems that are interconnected and have signals that are transferred from one sub-system to another. How this occurs in terms of the function of each block needs to be explained in the 'evaluation' section.

Design specifications should contain a range of both qualitative and quantitative terms based on their analysis of the problem and contain detailed realistic electronic parameters. A common misconception was to identify sub-systems and/or components as part of the specification. The choice of a particular sub-system/component may be part of the design solution to a problem but would not normally be part of the specification.

Alternative subsystems tended to be simply mentioned in many cases. At the very least, a circuit diagram needs to be included with some predictions of behaviour and reasons given for choice of subsystem. The better candidates also investigated the circuit behaviour of the alternatives.

A significant number of candidates provided extensive photographic evidence showing voltmeter readings at various stages of system development. Although this is useful, it should be considered as a supplement to tabulated results rather than an alternative. Often, even tabulated test results had very little analysis.

The physical circuit layout produced by most candidates was of a very good standard with the majority of circuits constructed very neatly on breadboard.

Task marking
Comments on approaches to internal marking

The assessment of the work was within tolerance in the vast majority of centres but in a small number of centres adjustments to marks were required.

Annotation of candidates' work and mark schemes was quite limited. A large number of centres failed to provide any annotation on either task. At the very least, an indication on the mark scheme of which level descriptors were or were not achieved together with marks awarded would greatly aid the moderation process.

Candidates should focus on a problem to analyse to enable them to write a design specification based on a specific identified problem. Candidates should select their own focus for the tasks based on different problems and this is expected to produce a wide range of tasks within a centre. The range of tasks produced within centres was variable. In many centres candidates produced a very good range of tasks with some of the work being outstanding and demonstrating considerable innovation. In a very small number of centres all candidates produced similar projects.

Supporting you

Useful contacts and links

Our friendly subject team are on hand to support you between 8.30am and 5.30pm, Monday to Friday.
Tel: 029 2240 4254
Email: electronics@eduqas.co.uk
Qualification webpage: https://www.eduqas.co.uk/qualifications/electronics-as-a-level/

See other useful contacts here: Useful Contacts | Eduqas

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Please find details for all our courses here: https://www.eduqas.co.uk/home/professional-learning/

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[i] ***Please note that where overall performance on a question/question part was considered good, with no particular areas to highlight, these questions have not been included in the report.***