GCE AS

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Part of WJEC

WJEC Eduqas GCE AS in ELECTRONICS

ACCREDITED BY OFQUAL
DESIGNATED BY QUALIFICATIONS WALES

SPECIFICATION

Teaching from 2017
For award from 2018

Version 2 January 2019

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cbac

SUMMARY OF AMENDMENTS

Version	Description	Page number
2	'Making entries' section has been amended to clarify resit rules and carry forward of NEA marks.	30

WJEC Eduqas GCE AS in ELECTRONICS

For teaching from 2017
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GCE AS ELECTRONICS

SUMMARY OF ASSESSMENT

Component 1: Principles of Electronics **Written examination: 2 hours 30 minutes** **80% of qualification**
A mix of short answer and extended answer questions with some set in a practical context.
Component 2: System design and realisation tasks **Non-exam assessment** **20% of qualification**
Task 1 A design and realisation task to design a digital system to solve an identified problem, need or opportunity. **Task 2** A design and realisation task to test an analogue circuit against a specification. **Task 3** A design and program task to create a microcontroller system programed via a flowchart to solve an identified problem, need or opportunity.

This linear qualification will be available for assessment in May/June each year. It will be awarded for the first time in summer 2018.

Ofqual Qualification Number (listed on The Register): 603/0778/X

Qualifications Wales Designation Number (listed on QiW): C00/1174/8

GCE AS ELECTRONICS

1 INTRODUCTION

1.1 Aims and objectives

The WJEC Eduqas AS in Electronics provides a broad, coherent, satisfying and worthwhile course of study. It encourages learners to develop confidence in, and a positive attitude towards, electronics and to recognise its importance in their own lives and in today's technological society.

The WJEC Eduqas AS in Electronics will ensure that learners have the electronic and mathematical knowledge and electronic engineering skills to solve problems. This should enable learners to appreciate how many problems in society can be tackled by the application of the scientific ideas in the field of electronics using engineering processes. The scope and nature of the learner's study should be coherent and practical. The practical work enables learners to see the theoretical knowledge contained in the specification in action and to gain greater understanding of the knowledge in a practical context.

Studying WJEC Eduqas AS in Electronics enables learners to:

- develop essential scientific knowledge and conceptual understanding of the behaviour of electrical/electronic circuits
- develop and demonstrate a deep understanding of the nature, processes and methods of electronics as an engineering discipline
- develop competence and confidence in a variety of practical, mathematical and problem solving skills
- develop and learn how to apply observational, practical and problem-solving skills in the identification of needs in the world around them and the testing of proposed electronic solutions
- develop and learn how to apply creative and evaluative skills in the development and assessment of electronic systems to solve problems
- develop their interest in electronics, including developing an interest in further study and careers associated with electronics.

1.2 Prior learning and progression

Any requirements set for entry to a course following this specification are at the discretion of centres. It is reasonable to assume that many learners will have achieved qualifications equivalent to Level 2 at KS4. Skills in Numeracy/Mathematics, Literacy/English and Information and Communication Technology will provide a good basis for progression to this Level 3 qualification.

This specification builds on the knowledge, understanding and skills established at GCSE.

This specification provides a suitable foundation for the study of electronics or a related area through a range of higher education courses, progression to the next level of vocational qualifications or employment. In addition, the specification provides a coherent, satisfying and worthwhile course of study for learners who do not progress to further study in this subject.

This specification is not age specific and, as such, provides opportunities for learners to extend their life-long learning.

1.3 Equality and fair access

This specification may be followed by any learner, irrespective of gender, ethnic, religious or cultural background. It has been designed to avoid, where possible, features that could, without justification, make it more difficult for a learner to achieve because they have a particular protected characteristic.

The protected characteristics under the Equality Act 2010 are age, disability, gender reassignment, pregnancy and maternity, race, religion or belief, sex and sexual orientation.

The specification has been discussed with groups who represent the interests of a diverse range of learners, and the specification will be kept under review.

Reasonable adjustments are made for certain learners in order to enable them to access the assessments (e.g. candidates are allowed access to a Sign Language Interpreter, using British Sign Language). Information on reasonable adjustments is found in the following document from the Joint Council for Qualifications (JCQ): *Access Arrangements and Reasonable Adjustments: General and Vocational Qualifications.*

This document is available on the JCQ website (www.jcq.org.uk). As a consequence of provision for reasonable adjustments, very few learners will have a complete barrier to any part of the assessment.

2 SUBJECT CONTENT

This section outlines the knowledge, understanding and skills to be developed by learners studying WJEC Eduqas AS in Electronics.

Learners should be prepared to apply the knowledge, understanding and skills specified in a range of theoretical, practical, industrial and environmental contexts. Learners' understanding of the connections between the different aspects of the subject is a requirement of this specification. In practice, this means that learners will be required to draw together different areas of knowledge, skills and understanding from across the full course of study.

Practical work is an intrinsic part of this specification. It is vitally important in developing a conceptual understanding of many topics and it enhances the experience and enjoyment of electronics. The practical skills developed are also fundamentally important to learners going on to further study in electronics engineering and related subjects, and are transferable to many careers.

All content in the specification should be introduced in such a way that it enables learners to:

- develop scientific knowledge and conceptual understanding of the behaviour of analogue and digital electrical/electronic circuits including a wide range of electronic components
- develop an understanding of the nature, processes and methods of electronics as an engineering discipline to help answer questions about practical circuits
- be aware of new and emerging technologies
- develop and learn how to apply observational, practical, problem solving and evaluative skills to identify needs in the world and to propose and test electronic solutions
- progress to Level 4 qualifications or careers in electronics and engineering.

The specification content is organised in sections. Each section contains the following:

Overview – summarises the content of each topic.

Electronic skills – summarises how skills may be developed in the section.

Mathematical skills (where appropriate) – a summary of mathematical skills that should be developed in each topic. The mathematical statements in this section are part of the assessed content. All of the 'mathematical skills' in Appendix B are referred to at least once in one of these sections.

Calculators may be used in both written examinations and in the NEA tasks. Candidates are responsible for making sure that their calculators meet the relevant regulations for use in written examinations: information is found in the JCQ publication *Instructions for conducting examinations.*

Learners should be able to: – these statements clarify the breadth and depth of the content for each topic.

Five appendices provide further details about:

Appendix A – Equations in electronics
Appendix B – Mathematical requirements and exemplification
Appendix C – Electronic symbols
Appendix D – Independence in non-exam assessment (NEA) tasks
Appendix E – Assessment grids for non-exam assessment

2.1 Component 1

Principles of Electronics

Written examination: 2 hours 30 minutes
80% of qualification
120 marks

This component covers the following topics:

1. System synthesis
2. DC Electrical circuits
3. Input and output sub-systems
4. Energy and power
5. Semiconductor components
6. Logic systems
7. Operational amplifiers
8. Timing circuits
9. Sequential logic systems
10. Microcontrollers
11. Mains power supply systems

1. SYSTEM SYNTHESIS

Overview

This topic looks at how to represent systems in terms of inputs, processes, outputs and feedback. This will enable complex systems to be represented in terms of sub-systems to allow the communication of complex systems.

Electronic skills

This topic looks at how learners can describe electronic systems and how complex systems can be broken down into sub-systems. These skills will be used throughout the study of electronics.

Learners should be able to:

(a) recognise that electronic systems consist of inputs, processes and outputs and may include feedback

(b) represent complex systems in terms of sub-systems

(c) analyse and design system diagrams.

2. DC ELECTRICAL CIRCUITS

Overview

This topic covers basic circuit theory. It involves the study of the resistance of an electronic circuit and its relationship with current and potential difference. Resistors and capacitors connected in series and parallel are also explored.

Electronic Skills

This topic gives learners the opportunity to explore electronic circuits through mathematical analysis and practical testing. Learners also develops investigative approaches and practical work, including safe and correct use of equipment and components; keeping records; constructing circuits from circuit diagrams and connecting appropriate measuring instruments.

Mathematical Skills

There are a number of opportunities for the development of mathematical skills in this topic. These include: recognising and using expressions in decimal and standard form; estimating results; using calculators to find reciprocals; using an appropriate number of significant figures; making order of magnitude calculations; and changing the subject of an equation.

Learners should be able to:

(a) use standard circuit symbols to interpret and draw circuit diagrams

(b) define resistance R, as $R = \frac{V}{I}$, describe the effects of resistors in circuits and be able to use the equation $V = IR$

(c) use the equations to calculate the effective resistance of combinations of resistors connected in series and/or parallel

$R = R_1 + R_2 + ...$ resistors in series

$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + ...$ resistors in parallel

$R = \frac{R_1 R_2}{R_1 + R_2}$ two resistors in parallel

(d) analyse circuits (based on a single power supply) using Kirchhoff's laws and Thevenin's theorem

(e) select appropriate values of resistor from the E24 series

(f) define capacitance, C as $C = \frac{Q}{V}$

(g) explain how capacitors can be used to form the basis of timing circuits and use the equations to calculate the effective capacitance of capacitors in series and parallel

$$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2} + \ldots$$ capacitors in series

$$C = \frac{C_1 C_2}{C_1 + C_2}$$ two capacitors in series

$$C = C_1 + C_2 + \ldots$$ capacitors in parallel.

3. INPUT AND OUTPUT SUB-SYSTEMS

Overview

This topic covers how input components can be used to give systems useful information about their environment and the type of outputs the system can control.

Electronic skills

The topic provides learners with opportunities to explore input devices and their application in sensing using voltage divider circuits through practical testing and mathematical analysis. Learners also develop investigative approaches and practical work, including safe and correct use of equipment and components; keeping records; constructing circuits from circuit diagrams and connecting appropriate measuring instruments.

Mathematical skills

There are a number of opportunities for the development of mathematical skills in this topic. These include: recognising and using expressions in decimal and standard form; estimating results; using an appropriate number of significant figures; and changing the subject of an equation.

Learners should be able to:

(a) describe the use of photosensitive devices, ntc thermistors and switches in a voltage divider circuit to provide analogue signals

(b) determine experimentally, interpret and use characteristic curves for the above devices

(c) use the equation to calculate output voltages for a voltage divider

$$V_{OUT} = \frac{R_2}{R_1 + R_2} V_{IN}$$

(d) explain how a Schmitt inverter can be used to provide signal conditioning

(e) design and construct sensing circuits with photosensitive devices, ntc thermistors and switches

(f) describe the use of a buzzer, a loudspeaker, a motor, a solenoid, a relay; a mechanical actuator (servo) and a seven-segment display in a system.

4. ENERGY AND POWER

Overview

This topic studies power in DC and AC circuits and the relationship between potential difference, current and power.

Electronic skills

This topic gives learners the opportunity to explore the power in a circuit through mathematical analysis for DC and AC circuits, with the use of rms (root mean square) voltages and current for an AC circuit.

Mathematical skills

There are a number of opportunities for the development of mathematical skills in this topic. These include: recognising and using expressions in decimal and standard form; calculating squares and square roots; estimating results; finding arithmetic means; using an appropriate number of significant figures; and changing the subject of an equation.

Learners should be able to:

(a) recall that power is defined as the rate of doing work and use the relationship between energy, power and time $E = Pt$

(b) select and apply the rms voltage and current equations, $V_{rms} = \frac{V_0}{\sqrt{2}}$ and $I_{rms} = \frac{I_0}{\sqrt{2}}$, including power calculations in a sinusoidal AC circuit

(c) use the power relationships $P = VI = I^2R = \frac{V^2}{R}$ for AC and DC circuits.

5. SEMICONDUCTOR COMPONENTS

Overview

This topic covers the construction of semiconductors in terms of n-type and p-type materials and the processes at a p-n junction and looks at the use of a range of diodes and transistors.

Electronic skills

The topic gives learners the opportunity to explore the action of several types of diodes and npn bipolar and MOSFET transistors. Learners will also work with various semiconductor devices and calculate values using component data and graphs.

Mathematical skills

There are a number of opportunities for the development of mathematical skills in this topic. These include: recognising and using expressions in decimal and standard form; estimating results; using an appropriate number of significant figures; changing the subject of an equation; and translating information between graphical, numerical and algebraic forms.

Learners should be able to:

(a) describe the use of light-emitting diodes, silicon diodes and zener diodes in electronic systems

(b) carry out relevant calculations on circuits containing these devices using data, including interpreting and sketching characteristic graphs including calculating series resistor values for LED circuits and selecting appropriate zener diodes

(c) describe the use of n-channel enhancement mode MOSFETs and npn bipolar transistors in switching circuits, using data to select suitable components for circuits

(d) define g_M as the gradient of an I_D-V_{GS} graph

(e) select and apply the equations

$I_C = h_{FE} I_B$ bipolar transistor

$I_D = g_M (V_{GS} - 3)$ MOSFET

$P = I_D^2 r_{DSon}$ power dissipated in a MOSFET.

6. LOGIC SYSTEMS

Overview

This topic studies the use of logic gates in control. The topic will look at the types of logic gates and their function, develop combinations of logic gates to perform other logic functions and to solve set tasks. Methods for simplifying logic systems will also be developed.

Electronic skills

This topic involves learners exploring the use of logic to control systems. The learner will work with different types of logic gates, learn how to connect and combine them to create different functions. They will use several methods to examine the workings of logic systems and be able to simplify the system.

Mathematical skills

There are a number of opportunities for the development of mathematical skills in this topic. These include: recognising and using expressions in Boolean algebra; simplifying logic systems using Boolean algebra, Karnaugh maps and multiplexers; and translating information between graphical, numerical and algebraic forms.

Learners should be able to:

(a) identify and use NOT; 2 and 3-input AND, NAND, OR, NOR, XNOR and XOR logic gates

(b) construct, recognise and use truth tables for these gates and simple combinations of them

(c) use combinations of one or more types of gate to perform other logic functions including NAND-gate simplification

(d) simplify logic systems using Boolean algebra, Karnaugh maps and multiplexers

(e) design and construct circuits containing logic gates, with consideration to sourcing, sinking, pull-up and pull-down resistors

(f) use de Morgan's theorem to simplify a logic system

$$\overline{A+B} = \overline{A}.\overline{B}$$

$$\overline{A.B} = \overline{A}+\overline{B}$$

(g) use the Boolean identities

$$A.1=A,\ A.0=0,\ A.A=A,\ A.\overline{A}=0,\ A+1=1,\ A+0=A,\ A+A=A,\ A+\overline{A}=1$$

(h) select and apply the Boolean identities

$$A+\overline{A}.B = A+B$$

$$A.B+A = A.(B+1) = A$$

7. OPERATIONAL AMPLIFIERS

Overview

This topic develops the uses of operational amplifiers (op-amp) and how they can be connected for different purposes. It involves the study of gain and outputs calculated from different inputs and resistor values and looks at bandwidth, distortion and slew-rate.

Electronic skills

This topic gives learners the opportunity to explore the different types of op-amps through modelling or simulation and to compare results to expected estimations and calculated results.

Mathematical skills

There are a number of opportunities for the development of mathematical skills in this topic. These include: recognising and using expressions in decimal and standard form; understanding and using the symbols: =,<,<<,>>,>,≈,Δ; estimating results; using an appropriate number of significant figures; making order of magnitude calculations; translating information between graphical and numerical form; interpreting data presented in graphical form; and changing the subject of an equation.

Learners should be able to:

(a) recall the characteristics of an ideal op-amp and be aware that these may be different for a typical op-amp

(b) recognise that the voltage difference between the two inputs of an op-amp with negative feedback is virtually zero (resulting in a virtual earth if one of the inputs is at 0 V) provided the output is not saturated

(c) explain the use of an op-amp in a comparator circuit

(d) recall how the output state of a comparator depends upon the relative values of the two input states and design comparator switching circuits

(e) recall and apply the conditions for the balance of a bridge circuit

(f) define the voltage gain, G, of an amplifier as $G = \frac{V_{OUT}}{V_{IN}}$ and be able to select and apply the equation

(g) draw, recognise and recall the characteristics of the following op-amp circuits,
- non-inverting amplifier
- inverting amplifier
- summing amplifier
- comparator
- voltage follower circuit

(h) select and apply the following equations for op-amp circuits:

- non-inverting amplifier $G = 1 + \frac{R_F}{R_1}$
- inverting amplifier $G = -\frac{R_F}{R_{IN}}$
- summing amplifier $V_{OUT} = -R_F\left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + ...\right)$

(i) select and apply the following equations for op-amp circuits:

- comparator $V_{OUT} = V_S \text{ for } V_+ > V_-$
  $V_{OUT} = -V_S \text{ for } V_+ < V_-$
- voltage follower circuit $V_{OUT} = V_{IN}$

(j) relate the input impedance of an op-amp to its configuration

(k) recall that the bandwidth is the frequency range over which the voltage gain is greater than $\frac{1}{\sqrt{2}}$ of its maximum value and estimate this bandwidth from a frequency response curve and use the gain-bandwidth product (unity gain bandwidth) to estimate bandwidth

(l) design single stage amplifiers based on inverting and non-inverting voltage amplifiers to achieve a specified voltage gain or bandwidth;

(m) explain how clipping and slew-rate can lead to distortion

(n) select and apply the equations

$\text{slew rate} = \frac{\Delta V_{OUT}}{\Delta t}$ definition of slew rate

$\text{slew rate} = 2\pi f V_P$ minimum slew-rate for distortion of free sinusoidal signal.

8. TIMING CIRCUITS

Overview

This topic develops the use of RC circuits to create time delays and their use in the creation of mono and astable timing circuits.

Electronic skills

This topic gives the learner opportunities to explore the charging and discharging of a RC network and its application in debouncing switches. Learners investigate the operation of a 555 timer IC in monostable and astable circuits through calculation, modelling and simulation. They will also study astable circuits based upon Schmitt triggers.

Mathematical skills

There are a number of opportunities for the development of mathematical skills in this topic. These include: recognising and using expressions in decimal and standard form; using an appropriate number of significant figures; changing the subject of an equation; substituting numerical values into algebraic equations using appropriate units for physical quantities; using calculators to find and use power, exponential and logarithmic functions; solving simple algebraic equations; translating information between graphical, numeric and algebraic form; plotting two variables from experimental or other data; interpreting and plotting logarithmic plots; interpreting data presented in graphical form; and changing the subject of an equation.

Learners should be able to:

(a) use the equation for the time constant (T) for an RC circuit: $T = RC$

(b) select and apply the exponential charging and discharging equations:

$$V_C = V_0\left(1 - e^{-\frac{t}{RC}}\right)$$ for a charging capacitor

$$V_C = V_0 e^{-\frac{t}{RC}}$$ for a discharging capacitor

and use 0.69 RC as the half time and 5 RC as an approximation to estimate effective charging and discharging times

(c) select and apply the equations

$$t = -RC\ln\left(1 - \frac{V_C}{V_0}\right)$$ charging capacitor

$$t = -RC\ln\left(\frac{V_C}{V_0}\right)$$ discharging capacitor

(d) calculate values of T, R and C for a charging / discharging capacitor by using a graph (including log graphs)

(e) use a RC circuit in debouncing switches

(f) recall the properties of monostable circuits

(g) explain the use of a monostable circuit in conjunction with a RC network in a time-delay circuit

(h) recall the properties of an astable circuit and its use as a pulse generator

(i) explain the operation, draw and design the circuit of an astable circuit based upon a Schmitt trigger and select and apply the approximation $f \approx \frac{1}{RC}$, where f is the operating frequency

(j) draw and analyse circuits for monostable and astable circuits based upon a 555 timer IC, and select and apply the following equations to calculate their characteristics including pulse duration, frequency, mark-space ratio

$f = \frac{1}{T}$	frequency, period relationship
$T = 1.1RC$	555 monostable
$t_H = 0.7(R_1 + R_2)C$	mark time of a 555 astable circuit
$t_L = 0.7R_2C$	space time of a 555 astable circuit
$f = \frac{1.44}{(R_1 + 2R_2)C}$	frequency of a 555 astable circuit
$\frac{T_{ON}}{T_{OFF}} = \frac{R_1 + R_2}{R_2}$	mark/space ratio of an astable.

9. SEQUENTIAL LOGIC SYSTEMS

Overview

This topic covers latches based on NAND gates and propagation delays in sequential systems. It involves the study of characteristics and uses for a range of systems based on D-type flip-flops, dedicated 4-bit counters, 2 digit decimal counter and synchronous counter systems.

Electronic skills

This topic expands on the logic systems topics, which gives the learners further opportunities to design and analyse sequential logic systems. Learners will also explore a range of uses for D-type flip-flops.

Mathematical skills

There are a number of opportunities for the development of mathematical skills in this topic. These include: recognising and using expressions in Boolean algebra; simplifying logic systems using Boolean algebra, Karnaugh maps and multiplexers; translating information between graphical, numerical and algebraic forms, constructing; and using timing diagrams and converting between binary, decimal, hexadecimal and binary-coded decimal (BCD) number systems.

Learners should be able to:

(a) design and describe the action of a Set-Reset ($\overline{\text{S}}\overline{\text{R}}$) latch based on NAND gates

(b) describe the significance of propagation delays in sequential systems

(c) construct and use timing diagrams to explain the operation of sequential logic circuits

(d) recall the characteristics and uses of the inputs and outputs of D-type flip-flops for:
- transition gates
- frequency divider circuits
- asynchronous counters

(e) design systems that use a dedicated 4-bit counter and combinational logic to produce a sequence of events

(f) design and analyse a 2 digit decimal counting system

(g) convert between binary, decimal, hexadecimal and binary-coded decimal (BCD) number systems.

10. MICROCONTROLLERS

Overview

This topic covers the microcontroller as a programable integrated circuit (PIC). It also covers how microcontrollers are interfaced and programed through flowcharts to perform tasks.

Electronic skills

Learners will have the opportunity in this topic to work with microcontrollers, interfacing them to inputs and outputs and programing them to perform set tasks. The learner will use flowcharts to program the microcontrollers. Learners will also look at the application of microcontrollers.

Mathematical skills

There are some opportunities for the development of mathematical skills in this unit. These include: converting between binary and decimal number systems; and drawing and interpreting flowcharts.

Learners should be able to:

(a) analyse and design flowchart programs to program microcontrollers.

11. MAINS POWER SUPPLY SYSTEMS

Overview

This topic explores power supplies with half and full wave rectification, the use of capacitors and load and line regulation. The topic also involves the analysis and design of regulators based upon a zener diode.

Electronic skills

This topic gives learners opportunities to model and simulate half and full wave rectification, by examining the effect of capacitors and loads on the output of simple power supplies. Learners can also construct and test a range of voltage regulators consisting of a zener diode, a transistor emitter follower or non-inverting amplifier.

Mathematical skills

There are a number of opportunities for the development of mathematical skills in this topic. These include: recognising and using expressions in decimal and standard form; using an appropriate number of significant figures; making order of magnitude calculations; changing the subject of an equation; translating information between graphical and numerical form; and interpreting data presented in graphical form.

Learners should be able to:

(a) recall the use of diodes for half-wave and full wave rectification

(b) describe the effect of capacitors and loads on the output of a simple power supply

(c) select and apply the ripple voltage equation

$$V_r = \frac{I}{f_r C}$$

(d) design zener-regulated power supplies and draw graphs to show the effect of loading.

2.2 Component 2

System design and realisation tasks
Non-exam assessment (NEA)

20% of qualification
60 marks

The NEA is an integral part of the WJEC Eduqas AS in Electronics and contributes 20% to the final assessment. This component requires each learner to complete three tasks independently. The tasks build on the concepts studied throughout the specification and the requirement to relate practical circuit design and realisation gained from the study of Component 1.

Task 1 (20 marks) – involves the development of a digital system.

Task 2 (20 marks) – involves the development and investigation to test an analogue system.

Task 3 (20 marks) – involves the development of a microcontroller system programed via a flowchart.

This component requires learners, in the context of the knowledge and understanding in Component 1, to demonstrate their ability to:

(a) analyse a problem[1] to enable solutions to be developed

(b) develop a design specification to solve a problem

(c) propose an electronic system, composed of sub-systems, to satisfy a design specification

(d) make predictions about the way that electronic systems behave

(e) design and build an electronic system, modelling its performance against the design specification, modifying as appropriate

(f) plan tests to make measurements, to explore a problem, selecting appropriate techniques and instruments

(g) evaluate practical risks in system development and application

(h) carry out tests having due regard to the correct manipulation of apparatus, accuracy of measurement and Health and Safety considerations

(i) make and record measurements on electrical circuits

(j) report results using standard scientific conventions

[1] In the context of AS electronics skills, 'problem' is interpreted broadly, to embrace:
- problem – difficulties in a situation e.g. a person with partial hearing cannot hear the doorbell
- context – looking at situations for possible design openings e.g. a person crossing the road
- opportunity – possibilities arising e.g. from a new improved component

(k) evaluate the performance of the electronic system against the design specification

(l) suggest improvements to the electronic system following evaluation

(m) design a microcontroller system; programming the microcontroller using a flowchart program (Task 3 only)

Learners should be encouraged and supported to select tasks in which they are interested and which are neither under nor over ambitious. The focus for each learner's task must be signed off by the teacher. The teacher should discuss the proposed focus of the task with the learner, considering the requirements of the assessment and the ability and interests of the individual learner. The teacher must be satisfied that the suggested focus has the potential for the individual learner to:

- analyse the problem and derive a design specification;
- develop and test a range of sub-systems;
- develop, realise and test a final physical system;
- evaluate the final system against the design specification and suggest improvements.

This will help ensure the task is at a suitable level for the learner concerned and will provide that individual with a level of challenge that is appropriate to their abilities, in the context of the requirements of an AS in Electronics qualification.

Having decided on a context for each task, the learner should undertake appropriate research so that a list of performance parameters (specification) can be produced. It is expected that the specification will contain realistic numerical values against which the final performance of the work can be judged.

In each task the overall system should be developed as a number of sub-systems which can be individually and/or incrementally tested.

The learner should fully document the development of each task in a report. It is the evidence contained within this report and the system produced upon which each task should be marked and assessed. The report should contain evidence for each task of the following sections:

- System planning – including analysis of the problem and a design specification

- System development – including the development of the system in terms of sub-system, annotated circuit diagrams and description of testing each sub-system and the recording of results

- System realisation – including annotated block and circuit diagrams; evidence of layout planning; description of testing of complete systems and the recording of results

- Evaluation – including a detailed evaluation of the system against the design specification and suggestions for improvement.

The report should be presented in a logical order that is easy to read and understand. It should contain an acknowledgement of all sources of information and help. Photographs of the complete physical system must be included in the report.

In each task the system should be fully tested when the project is complete. The testing should be documented with results being displayed in tables and graphs,

where appropriate. These tests will enable the learner to assess the system and identify faults and limitations. The learner should then evaluate the final system against the design specification and suggest further developments.

Task 1

Task 1 requires learners to design and realise a digital system. Initial sub-systems may be simulated and tested on CAD programs or development boards to prove the sub-systems before final realisation of a physical circuit of the complete system for testing.

Task 2

Task 2 requires learners to investigate an analogue system by designing, realising and testing it. The task has an emphasis on the testing and recording of results for an analogue system to meet their test specification.

Task 3

Task 3 is intended to introduce learners to software control techniques using flowcharts. Several manufacturers produce PIC development systems which can be used to deliver this part of the component. The work must not be limited to 'onscreen' design and emulation, but must involve the actual programing of a PIC chip, and its testing remotely on a physical circuit. Initial program testing can be carried out using a development board to prove the program before final testing on a physical circuit.

Physical circuit

Construction of all systems may be on prototype board, strip board or printed circuit board. Whichever method of construction is chosen, the layout and mounting of components and wiring should be neat and logical, assist the design, allow testing of and fault finding of the system. Pre-constructed circuit boards such as PIC or Arduino development boards are **not** acceptable as the final circuit.

Supervision

The tasks must be appropriately supervised to ensure that teachers are able to confidently authenticate each learner's work. Learners are allowed supervised access to resources that may include information gathered outside supervised time. Each learner must produce their NEA under immediate supervision.

Each learner must produce their system under 'immediate supervision'. This means the system has to be produced either:

(i) with the simultaneous physical presence of the learner and the supervisor,

or

(ii) remotely by means of simultaneous electronic communication.

In most cases supervision will be of the form described in (i), but in some circumstances, for example if the learner is carrying out a specialist process away from the centre, (ii) may be more appropriate.

Appendix D gives guidance on the level of independence in NEA tasks.

Time allocation

The NEA is integral to WJEC Eduqas AS Electronics and contributes 20% to the overall final assessment. Time is not prescribed for this work because the process of the learner's independent design and realisation tasks is iterative. They include the design, prototyping, testing and evaluating of sub-systems and systems, alongside the writing of the task reports. Learners should seek guidance from their teachers and engage as necessary in learner-led discussions. Teachers should make time available for the following:

- to explain the requirements of the independent design and construction task
- to guide learners to appropriate contexts
- to direct learners to the assessment objectives relevant to the assessment for the component
- to analyse Health and Safety considerations and the risk assessment of practical work.

As a consequence, the overall time allocated to the independent design and realisation tasks both by teacher and learners should be commensurate with a **20% weighting** of the whole qualification for this component.

3 ASSESSMENT

3.1 Assessment objectives and weightings

Below are the assessment objectives for this specification. Learners must be able to:

AO1
Demonstrate knowledge and understanding of the ideas, techniques and procedures of electronics

AO2
Apply knowledge and understanding of the ideas, techniques and procedures of electronics

AO3
Analyse problems and design, build, test and evaluate electronic systems to address identified needs

The table below shows the weighting of each assessment objective for each component and for the qualification as a whole.

	AO1	AO2	AO3	Total
Component 1	35%	35%	10%	80%
Component 2	-	-	20%	20%
Overall weighting	35%	35%	30%	100%

For each series, the weighting for the assessment of mathematical skills will be a minimum of 30% of the whole qualification.

Where appropriate learners will be expected to provide extended responses which are of sufficient length to allow them to demonstrate their ability to construct and develop a sustained line of reasoning which is coherent, relevant, substantiated and logically structured.

3.2 Arrangements for non-exam assessment

Marking of system design and realisation tasks

Marks should be awarded for the criteria listed in the assessment grids for non-exam assessment (see Appendix E).

Exemplification statements are given in the mark grid to indicate the features which should be present in a candidate's work to be awarded full marks for that section and the level.

A 'level of response' mark scheme is used. The relevant section(s) of the candidate's work should be read from start to finish before applying the mark scheme. Then the work should be matched to the level descriptors to decide which descriptor matches best with the candidate's work, whilst remembering to consider the overall quality of the response. Next, which mark to award within the band needs to be determined. If there is a good match with the content (and, where relevant, the communication statements for QER) then the highest mark for the band should be awarded. Lower marks within the band should be awarded for proportionately weaker matches with the content for the band.

It is the responsibility of the centre to ensure the authenticity of all work presented for assessment. All candidates are required to sign an authentication statement endorsing the originality of their work presented for assessment, and assessors must countersign that they have taken all reasonable steps to validate this. Authentication documentation must be completed by all candidates, not just those selected for moderation.

Marks should only be awarded for work which is that of the candidate. Any assistance that goes beyond general guidance must be recorded on the Electronics task form and taken into account when marking the work.

Marks should only be awarded when there is supporting evidence. Supervisors must annotate each candidate's Electronics task form and/or the relevant section of the work to identify the location of relevant evidence. Annotation should also be provided to indicate to what degree the final performance met the initial specification.

For each task the candidate's report must contain clear photographic evidence of the completed circuit.

The centre is responsible for carrying out internal standardisation where two or more teachers have been involved in the marking of the work submitted for a single unit.

Moderation of NEA

Once the centre has marked all candidates' work, the marks must be entered into the online system for each individual and sent electronically to WJEC. The online system will then select and return the candidates identified for the moderation sample.

For each candidate in the sample, the moderator must be sent a completed Electronics task form with the task reports and photographic evidence of the completed physical systems. The Electronics task form will be available on the WJEC website.

4 TECHNICAL INFORMATION

4.1 Making entries

This is a linear qualification in which all assessments must be taken at the end of the course. Assessment opportunities will be available in May/June each year, until the end of the life of this specification. Summer 2018 will be the first assessment opportunity.

A qualification may be taken more than once. Candidates must resit all examination components in the same series.

Marks for NEA may be carried forward for the life of the specification. If a candidate resits an NEA component (rather than carrying forward the previous NEA mark), it is the new mark that will count towards the overall grade, even if it is lower than a previous attempt.

Where a candidate has certificated on two or more previous occasions, the most recent NEA mark is carried forward, regardless of whether that mark is higher or lower (unless that mark is absent)The entry code appears below.

WJEC Eduqas AS in Electronics: B490QS

The current edition of our *Entry Procedures and Coding Information* gives up-to-date entry procedures.

4.2 Grading, awarding and reporting

Scaling factors may be applied to marks in order for them to achieve their intended weightings. In the case of WJEC Eduqas GCE AS in Electronics a scaling factor of 2 is applied to Component 1, with Component 2 remaining unscaled (i.e. it has a scaling factor of 1).

Component	Maximum raw mark	Scaling factor	Maximum scaled mark	% weighting
Component 1	120	2	240	80
Component 2	60	1	60	20

AS qualifications are reported as a grade from A to E. Results not attaining the minimum standard for the award will be reported as U (unclassified).

APPENDIX A

Equations in Electronics

In solving quantitative problems, learners should be able to correctly use the following relationships, using standard SI units, without them being provided:

$V = IR$	definition of resistance
$P = VI = I^2R = \frac{V^2}{R}$	power relationships
$R = R_1 + R_2 + ...$	resistors in series
$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} + ...$	resistors in parallel
$R = \frac{R_1 R_2}{R_1 + R_2}$	two resistors in parallel
$V_{OUT} = \frac{R_2}{R_1 + R_2} V_{IN}$	potential divider
$E = Pt$	energy transfer
$A.1=A$, $A.0=0$, $A.A=A$, $A.\overline{A}=0$ $A+1=1$, $A+0=A$, $A+A=A$, $A+\overline{A}=1$	Boolean identities
$\overline{A+B} = \overline{A}.\overline{B}$	de Morgan's theorem
$\overline{A.B} = \overline{A}+\overline{B}$	de Morgan's theorem

In addition, learners should be able to correctly select from a list and apply the following relationships:

$C = \frac{Q}{V}$	capacitance
$\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$	capacitors in series
$C = \frac{C_1 C_2}{C_1 + C_2}$	two capacitors in series
$C = C_1 + C_2$	capacitors in parallel

$$A + \overline{A} . B = A + B$$

$$A . B + A = A . (B + 1) = A$$ Boolean identities

$$G = \frac{V_{OUT}}{V_{IN}}$$ amplifier voltage gain

$$G = 1 + \frac{R_F}{R_1}$$ non-inverting op-amp circuit voltage gain

$$G = -\frac{R_F}{R_{IN}}$$ inverting op-amp circuit voltage gain

$$\text{slew rate} = \frac{\Delta V_{OUT}}{\Delta t}$$ definition of slew rate

$$\text{slew rate} = 2\pi f V_P$$ minimum slew rate for distortion of free sinusoidal signal

$$V_{OUT} = -R_F \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + ... \right)$$ summing amplifier output voltage

$$V_{OUT} = V_S \text{ for } V_+ > V_-$$ comparator output voltage
$$V_{OUT} = -V_S \text{ for } V_+ < V_-$$

$$V_{OUT} = V_{IN}$$ voltage follower circuit

$$T = RC$$ time constant

$$V_C = V_0 \left(1 - e^{-\frac{t}{RC}} \right)$$ charging capacitor

$$t = -RC \ln \left(1 - \frac{V_C}{V_0} \right)$$ charging capacitor

$$V_C = V_0 e^{-\frac{t}{RC}}$$ discharging capacitor

$$t = -RC \ln \left(\frac{V_C}{V_0} \right)$$ discharging capacitor

$$V_{rms} = \frac{V_0}{\sqrt{2}} ; \; I_{rms} = \frac{I_0}{\sqrt{2}}$$ rms values

$I_C = h_{FE} I_B$	bipolar transistor
$I_D = g_M (V_{GS} - 3)$	MOSFET
$P = I_D^2 r_{DSon}$	power dissipated in a MOSFET
$f = \frac{1}{T}$	frequency, period relationship
$T = 1.1RC$	555 monostable
$t_H = 0.7(R_1 + R_2)C$	mark time of a 555 astable circuit
$t_L = 0.7R_2C$	space time of a 555 astable circuit
$f = \frac{1.44}{(R_1 + 2R_2)C}$	frequency of a 555 astable circuit
$\frac{T_{ON}}{T_{OFF}} = \frac{R_1 + R_2}{R_2}$	mark/space ratio of an astable
$f \approx \frac{1}{RC}$	Schmitt astable circuit
$V_r = \frac{I}{f_r C}$	ripple voltage

APPENDIX B

Mathematical requirements and exemplification

In order to be able to develop their skills, knowledge and understanding in electronics, learners need to have been taught, and to have acquired competence in the following areas of mathematics indicated in the table below.

The table illustrates where these mathematical skills may be developed and could be assessed. The list of examples is not exhaustive. These skills could also be developed in other areas of the specification content.

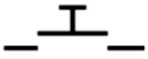
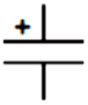
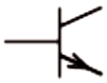
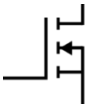
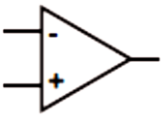
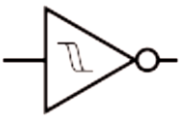
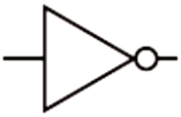
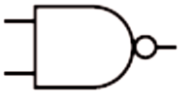
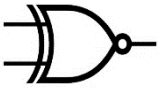
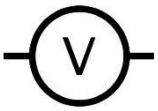
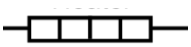
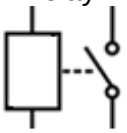
	Mathematical skill	**Exemplification of mathematical skill (assessment is not limited to the examples given below)**
E.0 – arithmetic and numerical computation		
E.0.1	Recognise and make use of appropriate units in calculations	Convert between units with different prefixes, e.g. A to mA Identify the correct units for physical properties such as Hz, the unit for frequency
E.0.2	Recognise and use expressions in decimal and standard form	Use frequencies expressed in standard form such as 2.5×10^7 Hz
E.0.3	Use fractions, ratios and percentages	Calculate the fraction of the charge lost from a capacitor in a given time
E.0.4	Estimate results	Estimate the resistor values needed in a potential divider so that the output voltage does not drop significantly
E.0.5	Use calculators to handle power functions, exponential and logarithm functions	Calculate the power rating required for a resistor Calculate the time constant from a decay curve
E.1 – handling data		
E.1.1	Use an appropriate number of significant figures	Report calculations to an appropriate number of significant figures Understand that calculated results can only be reported to the limits of the least accurate measurement
E.1.2	Find arithmetic means	Calculate a mean value for repeated experimental findings
E.1.3	Make order of magnitude calculations	Evaluate equations with variables expressed in different orders of magnitude, e.g. 150 kΩ and 2.6 mA
E.1.4	Use Karnaugh maps	simplify a logic system

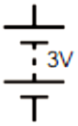
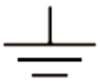
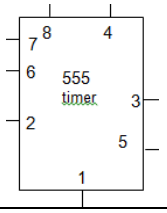
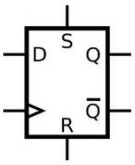
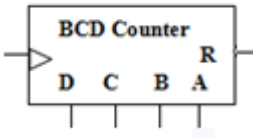
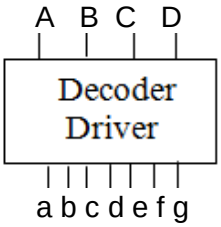
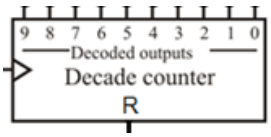
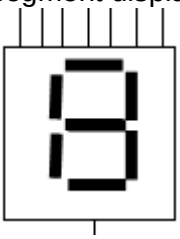
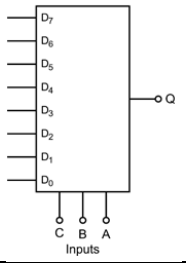
	Mathematical skill	**Exemplification of mathematical skill (assessment is not limited to the examples given below)**
E.2 – algebra		
E.2.1	Understand and use the symbols: =, <, <<, >, >>, $\propto$, $\approx$, Δ	Recognise the significance of the symbols in the expression: $\text{slew rate} = \frac{\Delta V_{OUT}}{\Delta t}$
E.2.2	Change the subject of an equation, including non-linear equations	Rearrange $P = \frac{V^2}{R}$ to make R the subject
E.2.3	Substitute numerical values into algebraic equations using appropriate units for physical quantities	Calculate the frequency of a 555 astable by substituting the values for R_1, R_2 and C into the equation: $f = \frac{1.44}{(R_1 + 2R_2)C}$
E.2.4	Solve algebraic equations	Find a capacitor value for a given time delay and resistance in a 555 monostable
E.2.5	Use Boolean algebra	Simplify a logic system
E.3 – graphs		
E.3.1	Translate information between graphical, numerical and algebraic forms	Measure the ripple voltage from output graphs for rectified power supplies
E.3.2	Plot two variables from experimental or other data	Plot V-I characteristics of a diode
E.3.3	Determine the slope of a graph	Calculate a resistance value from a V-I graph
E.3.4	Calculate the rate of change from a graph showing a linear relationship	Calculate the slew rate from a V-t graph
E.3.5	Draw and use the slope of a tangent to a curve as a measure of rate of change	Calculate the gain of an amplifier from the transfer characteristic
E.3.6	Sketch relationships which are modelled by $y = \sin x$ and $y = \sin^2 x$	Sketch a graph of power against time for an alternating current in a resistor

APPENDIX C

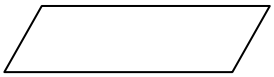
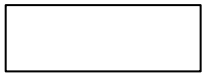
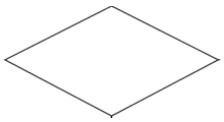
Electronic symbols

Learners should recognise and be able to use the following electronic symbols:

Switch (latching) 	Switch (non-latching) 	Light dependent resistor 	Thermistor 
Photodiode 	Microphone 	Variable resistor 	Potentiometer 
Resistor 	Capacitor 	Electrolytic capacitor 	Inductor 
NPN transistor 	PNP transistor 	N channel MOSFET 	Diode 
Zener diode 	Op-amp 	Schmitt inverter 	NOT gate 
AND gate 	OR gate 	NAND gate 	NOR gate 
XOR gate 	XNOR symbol 	Voltmeter 	Ammeter 
Buzzer 	Speaker 	Signal lamp 	Filament lamp 
Light emitting diode 	Heater 	Motor 	Relay 

Cell 	Battery 	AC supply 	Transformer 
Earth 	555 timer 	D type flip flop 	Binary counter 
Decoder driver 	Decade counter 	7 segment display 	Multiplexer 

Circles can be put on S and R inputs for D types, and on CK and R inputs for counters (or bars over the letters) when inverted.

Terminator 	Input/output 	Process 	Decision 

APPENDIX D

Independence in non-exam assessment tasks

The table below gives guidance on the level of independence that a learner must follow at each stage of the non-exam assessment (NEA) tasks.

Task stage	**Level of independence**	**What does this level of independence mean at this stage? (The following are examples.)**	**What are the potential risks?**	**What are the controls in place to mitigate these risks?**
Context for task	Independent work	Centres may give learners a free choice of focus for their task or provide learners with a theme or range of themes. However, it is not acceptable for learners to choose from a list of specific focuses provided by the centre. Learners may discuss together and with their teacher ideas for an appropriate focus for their tasks.	The parameters that the centre provides may not allow sufficient scope for learners to independently derive their own focus. The focus a learner chooses may not provide sufficient scope to allow them to access the full range of marks available for the NEA.	The guidance that teachers provide needs to ensure that the scope is sufficient for learners to arrive at the focus for their task independently. The viability of a learner's potential focus can be discussed with the teacher. Teacher to 'sign off' focus for project to ensure the proposed focus provides suitable scope for the learner. Any guidance that goes beyond general guidance must be recorded by the teacher on the Electronics task form and taken into account when the work is marked. For example, supplying learners with a focus for their task would be beyond general guidance.

Task stage	**Level of independence**	**What does this level of independence mean at this stage? (The following are examples.)**	**What are the potential risks?**	**What are the controls in place to mitigate these risks?**
System planning	Independent work	Learners independently carry out research and derive a specification for their task.	Learners plagiarise their work from others.	Teacher assessment of learners' work. Teacher and learner declarations state that the work is the learner's own. Any guidance that is beyond general guidance must be recorded on the Electronics task form and taken into account when the work is marked. For example, giving learners research material on a specific need for their task would be beyond general guidance. Moderators will be instructed to report any suspected instance of plagiarism or learners not working independently for further investigation.

Task stage	**Level of independence**	**What does this level of independence mean at this stage? (The following are examples.)**	**What are the potential risks?**	**What are the controls in place to mitigate these risks?**
System Development	Independent work	Learners independently plan and carry out testing of each sub-system for their system to meet their specification.	Learners plagiarise their work from others. Learners do not model their own sub-systems and test them.	There will be evidence of learners constructing and carrying out tests on sub-systems. Teacher assessment of learners' work. Teacher and learner declarations state that the work is the learner's own. Any guidance that is beyond general guidance must be recorded on the Electronics task form and taken into account when the work is marked. For example, showing learners how to interface two sub-systems for their task would be beyond general guidance. Moderators will be instructed to report any suspected instance of plagiarism or learners not working independently for further investigation.

Task stage	**Level of independence**	**What does this level of independence mean at this stage? (The following are examples.)**	**What are the potential risks?**	**What are the controls in place to mitigate these risks?**
System Realisation	Independent work	Learners independently plan and carry out the construction and testing of their complete system to meet their specification.	Learners plagiarise their work from others. Learners do not construct their own physical system and test it.	There will be evidence of learners constructing and carrying out tests on complete systems. Teacher's immediate supervision and assessment of learners' work. Teacher and learner declarations state that the work is the learner's own. Any guidance that is beyond general guidance must be recorded on the Electronics task form and taken into account when the work is marked. For example, showing learners how to test a system for their task would be beyond general guidance. Moderators will be instructed to report any suspected instance of plagiarism or learners not working independently for further investigation.

Task stage	**Level of independence**	**What does this level of independence mean at this stage? (The following are examples.)**	**What are the potential risks?**	**What are the controls in place to mitigate these risks?**
Evaluation	Independent work	Learners independently evaluate the performance of their complete system and suggest improvements.	Learners plagiarise their work from others.	Teacher assessment of learners' work. Teacher and learner declarations state that the work is the learner's own. Any guidance that is beyond general guidance must be recorded on the Electronics task form and taken into account when the work is marked. For example, supplying learners with points to discuss in the evaluation for their task would be beyond general guidance. Moderators will be instructed to report any suspected instance of plagiarism or learners not working independently for further investigation.

APPENDIX E

Assessment grids for non-exam assessment
System design and realisation tasks
Task 1: Digital system

1. System planning		**Band**
3 marks	**The candidate has provided**: • a clear analysis of a problem leading to a design specification in both qualitative and quantitative terms (typically at least 3 of each), and including 3 or more detailed realistic electronic parameters	3
2 marks	**The candidate has provided**: • some analysis of a problem with a design specification in qualitative and quantitative terms (typically at least 2 of each), and including 1 or more realistic electronic parameters	2
1 mark	**The candidate has provided:** • a limited analysis of a problem and a partial design specification in either qualitative or quantitative terms (typically at least 4 in total)	1
0 marks	Response not creditworthy or not attempted.	
2. System Development		**Band**
6 - 8 marks	**The candidate has:** • provided a clearly labelled block diagram for the system and developed the system as a series of sub-systems and made predictions regarding its behaviour • produced an accurate good quality fully labelled circuit diagram for the system • planned and produced a very well organised physical circuit layout with all wires arranged vertically/horizontally, and showed good awareness of risk assessment • arranged wires with no unnecessary crossing of components which were mounted to a high standard and showed good awareness of safe working procedures	3
3 - 5 marks	**The candidate has:** • provided a labelled block diagram for the system and made some attempt to develop the system as a series of sub-systems • produced an accurate well labelled circuit diagram for the system • planned and produced a generally well organised physical circuit layout with most wires arranged vertically/horizontally and showed some awareness of risk assessment • arranged most wires without unnecessary crossing of components which were mounted to a good standard and showed awareness of safe working procedures	2
1 - 2 marks	**The candidate has:** • made a superficial attempt to develop the system as a series of sub-systems • produced a circuit diagram for the system which was partially labelled or lacked clarity • produced a physical circuit layout with minimal evidence of organisation/planning and showed some superficial awareness of risk assessment/ safe working procedures	1
0 marks	Response not creditworthy or not attempted.	

3. System Realisation		**Band**
5 - 6 marks	**The candidate has:** • performed functional tests on all the sub-systems and recorded all relevant results • tested the complete physical system prototype and provided a detailed analysis of the results using standard scientific convention which included most of the relevant electrical measurements • produced an electronic system that worked consistently and reliably and included a comprehensive user guide	3
3 - 4 marks	**The candidate has:** • performed functional tests on most of the sub-systems and recorded most relevant results • tested the complete physical system prototype and provided some analysis of the results using standard scientific convention which included some of the relevant electrical measurements • produced an electronic system that worked most of the time and included a user guide	2
1 - 2 marks	**The candidate has:** • performed functional tests on 1 or more different sub-systems and made some attempt at recording the results • tested the complete physical system prototype and provided a limited analysis of the results • produced an electronic system in which at least 2 sub-systems worked most of the time	1
0 marks	Response not creditworthy or not attempted.	

4. Evaluation		**Band**
3 marks	**The candidate has:** • undertaken a critical and objective evaluation of the performance of the complete system which was valid, made comprehensive comparisons with the design specification and made at least 2 suggestions for improvement with explanations of how they improve the system	3
2 marks	**The candidate has:** • undertaken an objective evaluation of the performance of the complete system which was valid, made some comparisons with the design specification and made at least 2 suggestions for improvement	2
1 mark	**The candidate has:** • undertaken a simple evaluation of the performance of the complete system which was valid in few respects, made minimal comparison with the design specification and made at least 1 superficial suggestion for improvement	1
0 marks	Response not creditworthy or not attempted.	

Task 2: Analogue system

1. System planning		**Band**
3 marks	**The candidate has provided**: • a clear analysis of a problem leading to a design specification in both qualitative and quantitative terms (typically at least 3 of each), and including 3 or more detailed realistic electronic parameters	3
2 marks	**The candidate has provided**: • some analysis of a problem with a design specification in both qualitative and quantitative terms (typically at least 2 of each), and including 1 or more realistic electronic parameters	2
1 mark	**The candidate has provided:** • a limited analysis of a problem and a partial design specification in either qualitative or quantitative terms (typically at least 4 in total)	1
0 marks	Response not creditworthy or not attempted.	
2. System Development		**Band**
4 marks	**The candidate has:** • produced an accurate good quality circuit diagram for the system which was clearly labelled • planned and produced a very well organised physical circuit layout with all wires arranged vertically/horizontally, and showed good awareness of risk assessment	3
2 - 3 marks	**The candidate has:** • produced an accurate well labelled circuit diagram for the system • planned and produced a generally well organised physical circuit layout with most wires arranged vertically/horizontally and showed some awareness of risk assessment	2
1 mark	**The candidate has:** • produced a circuit diagram for the system that was partially labelled or lacked clarity • produced a physical circuit layout with minimal evidence of organisation/planning and showed some superficial awareness of risk assessment/ safe working procedures	1
0 marks	Response not creditworthy or not attempted.	

3. System Realisation		**Band**
8 - 10 marks	**The candidate has:** • provided comprehensive evidence of planning test procedures and has clearly identified all the appropriate test equipment and made predictions regarding test ranges required • tested the complete physical system prototype with all the relevant numerical measurements of the system parameters being made making, appropriate use of standard scientific convention • provided a detailed justification for the accuracy of most of the measurements made and clearly recorded the results in table form and graphically • provided a detailed analysis of the results	3
4 - 7 marks	**The candidate has:** • provided evidence of planning test procedures and has identified all the appropriate test equipment • tested the complete physical system prototype with most of the relevant numerical measurements of the system parameters being made, making some appropriate use of standard scientific convention • provided some justification for the accuracy of most of the measurements made and recorded the results in table form and graphically • provided good analysis of the results	2
1 - 3 marks	**The candidate has:** • provided minimal evidence of planning test procedures and has identified some appropriate test equipment • partially tested the complete physical system prototype and made basic numerical measurements • recorded results in table form or graphically • provided some analysis of the results	1
0 marks	Response not creditworthy or not attempted.	

4. Evaluation		**Band**
3 marks	**The candidate has:** • undertaken a critical and objective evaluation of the performance of the complete system which was valid, made comprehensive comparisons with the design specification and made at least 2 suggestions for improvement with explanations of how they improve the system	3
2 marks	**The candidate has:** • undertaken an objective evaluation of the performance of the complete system which was valid, made some comparisons with the design specification and made at least 2 suggestions for improvement	2
1 mark	**The candidate has:** • undertaken a simple evaluation of the performance of the complete system which was valid in few respects, made minimal comparison with the design specification and made at least 1 superficial suggestion for improvement	1
0 marks	Response not creditworthy or not attempted.	

Task 3: Microcontroller system (Flowchart program)

1. System planning		**Band**
2 marks	**The candidate has provided**: • a clear and concise analysis of a problem and a design specification in both qualitative and quantitative terms (typically at least 3 of each), and including two or more detailed realistic measurable parameters	2
1 mark	**The candidate has provided:** • An analysis of a problem and a partial design specification in either qualitative or quantitative terms (typically at least 4 in total)	1
0 marks	Response not credit worthy or not attempted	
2. System Development		**Band**
6 - 8 marks	**The candidate has:** • produced a comprehensive flowchart solution to the problem and make predictions regarding its behaviour • devised a program that reacted to and used information from inputs to control outputs and utilised 4 or more port bits • used 8 or more different commands in the program including two types of decision command • produced simulation tests and given a full account of the tests on the proposed flowchart program	3
3 - 5 marks	**The candidate has:** • produced a good flowchart solution to the problem • devised a program that reacted to and used information from inputs to control outputs and utilised 3 or more port bits • used 6 or more different commands in the program including one or more types of decision command • produced simulation tests and given a reasonable account of the tests on the proposed flowchart program with minor omissions in the results	2
1 - 2 marks	**The candidate has:** • produced a basic flowchart solution to the problem • devised a program that utilised 2 or more port bits • used 4 or more different commands in the program • produced simulation tests and given a superficial account of the tests on the proposed flowchart program, with some omissions in the results	1
0 marks	Response not creditworthy or not attempted	

3. System Realisation		**Band**
6 - 8 marks	**The candidate has:** • produced an accurate circuit diagram and physical circuit layout which were very well organised and provide a component list • made most wire connections and mounted most components to a high standard and showed good awareness of risk assessment/safe working procedures • downloaded the program to the microcontroller circuit and comprehensively tested the complete physical system prototype • provided a detailed analysis of the results for a system that worked consistently and reliably	3
3 - 5 marks	**The candidate has:** • produced an accurate circuit diagram and physical circuit layout which were organised • made most wire connections and mounted most components to a good standard and showed some awareness of risk assessment/safe working procedures • downloaded the program to the microcontroller circuit and tested the majority of the complete physical system prototype • provided some relevant analysis of the results with some detail for a system that mainly worked	2
1 - 2 marks	**The candidate has:** • produced a circuit diagram and physical circuit layout which tended not to be very well organised; • downloaded the program to the microcontroller circuit and partially tested the complete physical system prototype; • provided some superficial analysis of the results for a system that worked at some time.	1
0 marks	Response not creditworthy or not attempted	

4. Evaluation		**Band**
2 marks	**The candidate has:** • undertaken an objective evaluation of the performance of the complete system which was valid, made comprehensive comparisons with the design specification and made at least 2 suggestions for improvement with explanations of how they improve the system	2
1 mark	**The candidate has:** • undertaken a simple evaluation of the performance of the complete system which was valid in few respects, made minimal comparison with the design specification and made at least 1 superficial suggestion for improvement	1
0 marks	Response not creditworthy or not attempted	